ZYG SYSTEM BLOCK DIAGRAM

EV@ --- GPU
MV@ --- iGPU & GPU
N12P@ --- N12P-GS
N12E@ --- N12E-GE
SPG --- Special
GPS@ --- GPS
BT@ --- BT
SKU

+VCCSA TPS51461 P42	CHARGER ISL88731A P36
GPU CORE PWR MAX17007AGTI+ P43	3/5V SYS PWR RT8223M P37
GPU PWR P44	CPU CORE PWR MAX17511GTL+ P38
+1.8V, DT power HPA00835RTER P45	CPU VCC_GFX MAX17511GTL+ P39
THERMAL PROTECTION P46	VTT 1.05V RT8238A P40
+5V_ADO TPS51117RGYR P47	DDR3 PWR RT8207A P41

intel <MCH Processor>
Sandy Bridge
rPGA 989 (37.5mm X 37.5mm) P3,4,5,6
DDR SYSTEM MEMORY
FDI
DMI
PCI-E X16

BCLK: 100MHz
DPLL_REF_SSCLK: 120MHz

DDR III
SO-DIMM A0
SO-DIMM B0
SO-DIMM A1 (QC)
SO-DIMM B1 (QC)
P13, 14, 15, 16

Dual Channel
1333 MT/s
166 MT/s

VRAM
gDDR3 8pcs
(64*16 / 128*16)
P23~24

X'TAL 27.0MHz

nVIDIA GPU
N12E GE Package GB3-128
N12P GS Package GB2-128
Optimus (Muxless) P18~P22

PCIE

FDI interface
X4 DMI interface

intel <PCH>
FDI P7
DMI P7
Graphics Interfaces P7
SATA 6.0 GT/s
P8
SATA 3.0 GT/s
CougarPoint
mBGA 989 (27mm X 25mm) P7,8,9,10,11,12
PCI-E P9
USB P9
RTC P9
HDA P8
SPI
LPC P8

X'TAL 32.768KHz

Muxless LVDS — dGPU LVDS — **LVDS** P25
Muxless CRT — dGPU CRT — **CRT** P25
Muxless HDMI — dGPU HDMI — **HDMI** P26

SATA0 6GB/s — **HDD (SATA) *2** Floating type P27
SATA1 6GB/s
SATA5 3GB/s — **ODD (SATA)** Zero power ODD P27
SATA4 3GB/s

HM65 does not support USB 6 & 7

eSATA/USB Combo Conn. USB 9 (Debug) P32
eSATA Buffer P32
USB Port x 3 Dual way USB 3, 11, 12 (Debug) P32
Bluetooth USB 4 P34
CCD USB 8 P25
FingerPrint USB 2 P34
Detachable Touchpad USB 5 P17

USB 2.0

PCI-Express
PCIe port 2/CLK3 — **USB3.0 Chip** NEC UPD720200F1 P33 — **USB charger** MAX14566AE P33 — **USB 3.0 Conn .** USB 1 P33

PCIe port 5/CLK5 — **IEEE1394 & Media Cardreader** JM388A P31 — X'TAL 24.576MHz
IEEE1394a connector P31
Card Reader Connector P31

PCIe port 6/CLK1 — **Mini Card WLAN** USB 10 1H P28
PCIe port 3/CLK2 — **Mini Card GPS** USB 13 1F/H P28

PCIe port 1/CLKB
Realtek Giga-LAN RTL8111E P34 & Daughter Board — X'TAL 25MHz
Transformer Daughter Board
RJ45 Connector Daughter Board
P32

Azalia
Audio CODEC ALC669X P29
SPI ROM P8
EC WPCE791L P35
SPI ROM P35

Surround Stereo Amp (G1453L/ 2W+2W) P30
Center Mono Amp (G1442/ 2W) P29
Front Audio Amp & Head phone AN12947A P30
Sub-Amplifier (TPA3111D1) P30

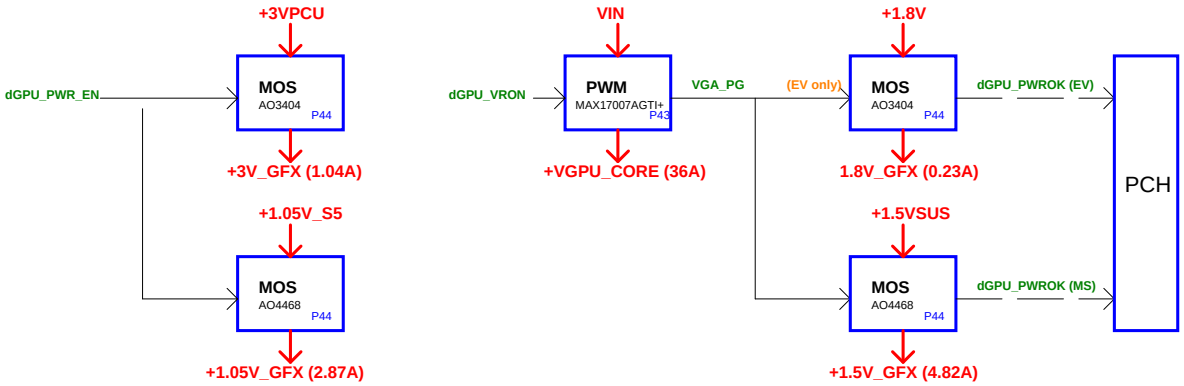
Surround Speaker X2 P30
Center Speaker P30
Speaker X2 P30
S/PDIF P30
SUBWOOFER P30
Line in P30
MIC Jack P30
Int. D-MIC P30
K/B CON. Backlit P34

Quanta Computer Inc.
PROJECT : ZYG

Size	Document Number	Rev
	ZYG Block Diagram	1A

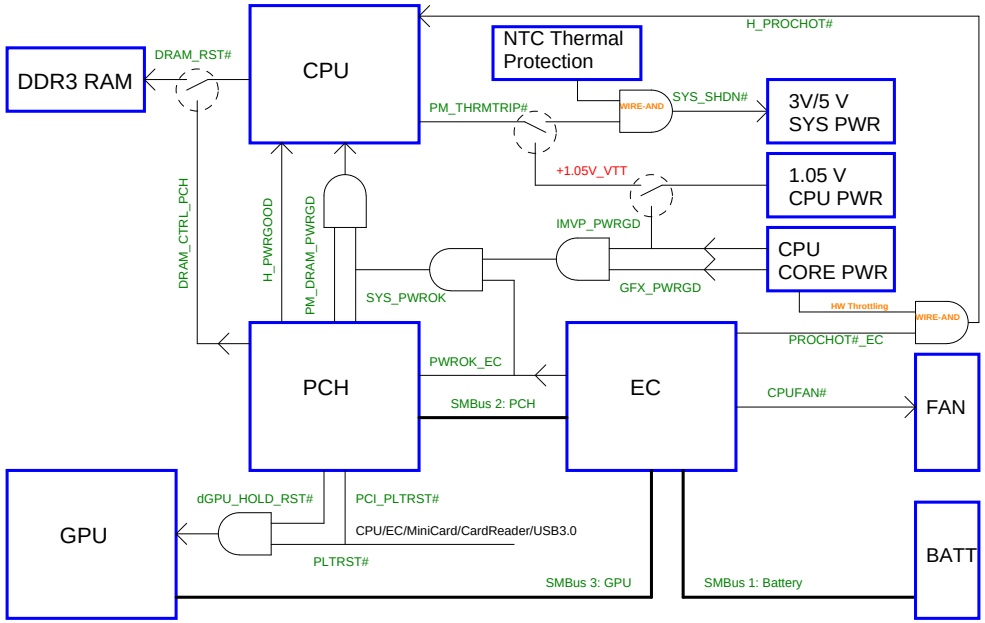
Date: Friday, February 18, 2011 Sheet 1 of 50

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	DDR3 RAM POWER	SUSON	S0-S3
+SMDDR_REF	+0.75V	SODIMM Reference Voltage	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/POWER	MAINON	S0
+1.8V	+1.8V	CPU/PCH POWER	MAINON	S0
+1.05V_S5	+1.05V	CPU/SODIMM CORE POWER	S5_ON	S0-S5
+1.05V_VTT	+1.05V	CPU VTT POWER	MAINON	S0
+1.05V_PCH	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
+VCC_GFX	variation	SNB GRAPHIC POWER	VR_ON	S0
+VCCSA	+0.8/0.9V	CPU SYSTEM ANGENT AGENT	VTT_HWPG	S0
+1.05V_GFX	+1.05V	GPU IO/PLL POWER	dGPU_PWR_EN	Discrete enable
+3V_GFX	+3.3V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN	Discrete enable
+VGPU_CORE	+0.8125V~+1V	GPU CORE POWER	dGPU_VRON	Discrete enable
+1.5V_GFX	+1.5V	VRAM CORE POWER	VGA_PG	Discrete enable
+1.8V_GFX	+1.8V	GPU_CRE/LVDS/PLL POWER	VGA_PG	Discrete enable
+5V_ADO	+5V	AUDIO CODEC AMPLIFIER	MAINON	S0
+5V_DT	+5V	DT CHARGING	DT_CHG	TBD



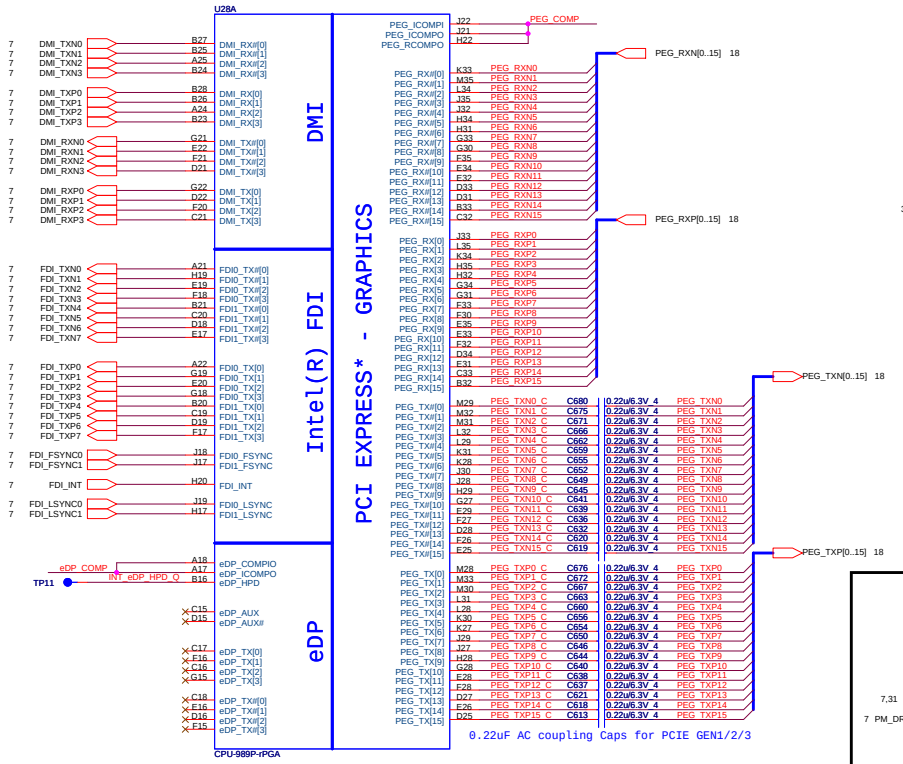
Quanta Computer Inc.

PROJECT : ZYG

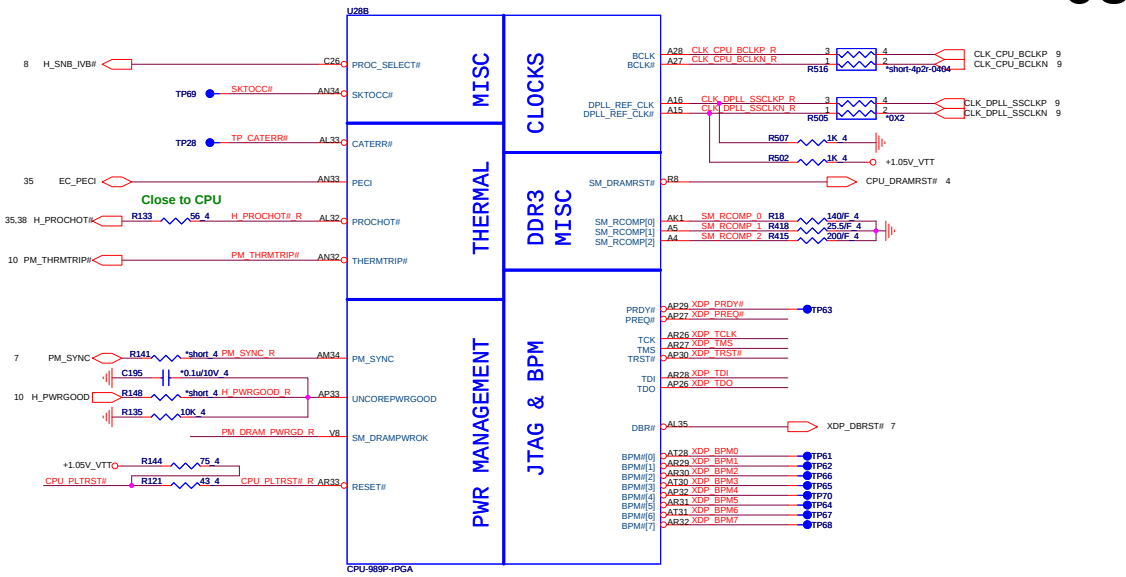
Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

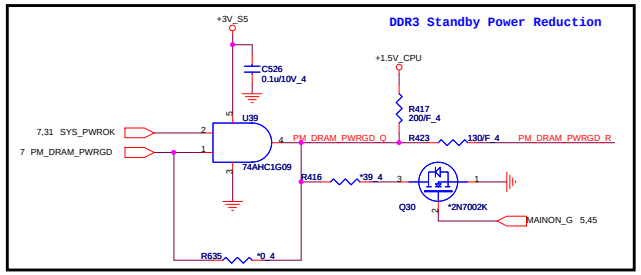
Date: Tuesday, December 14, 2010 Sheet 2 of 50

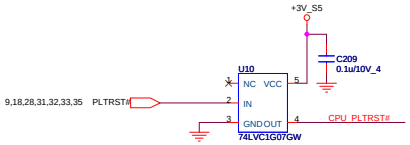
Sandy Bridge Processor (DMI,PEG,FDI)



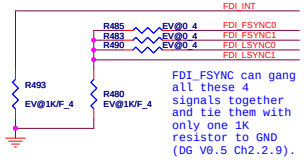
Sandy Bridge Processor (CLK,MISC,JTAG)





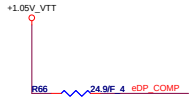


FDI Disabling (Discrete Only)



FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

DP & PEG Compensation

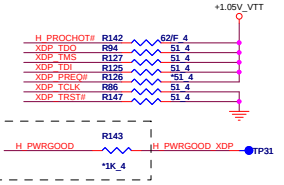


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

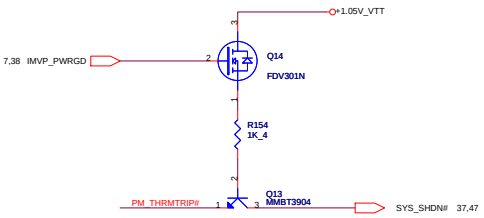
PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)



H_PWRGOOD need very short from process to 1K



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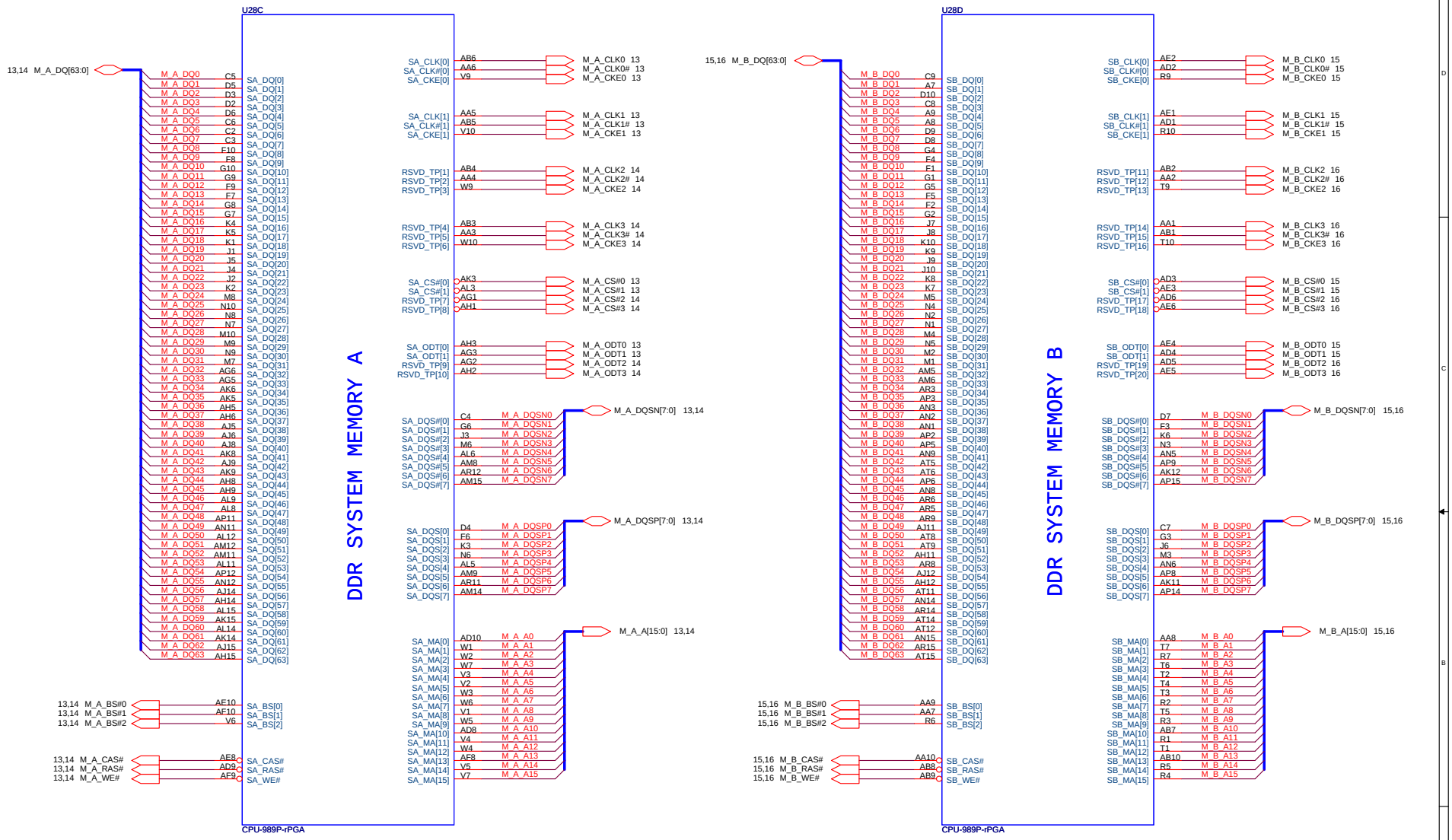
PROJECT : ZYG

Size	Document Number	Rev
	Sandy Bridge 1/4	1A

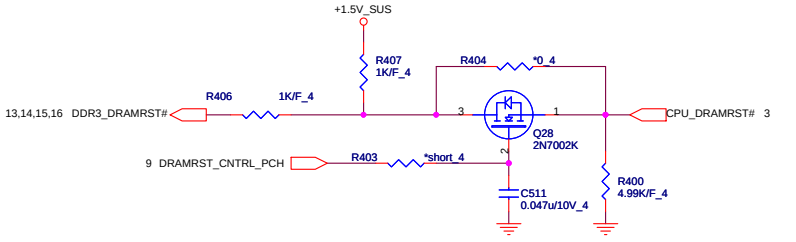
Date: Tuesday, February 22, 2011 Sheet 3 of 50

Sandy Bridge Processor (DDR3)

04



DDR3 Standby Power Reduction



Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	Sandy Bridge 2/4	1A

Date: Tuesday, February 22, 2011 Sheet 4 of 50

Sandy Bridge Processor (POWER)

CPU VTT SNB 45W : 8.5A

Spec	Real
330uF/6mohm x 2	390uF/10mohm x 1
22uF x 12	22uF x 10
22uF x 7 (Non-stuff)	10uF x 3

CPU VGT SNB 45W : 33A

Spec	Real
470uF/4mohm x 2	330uF/10mohm x 1
22uF x 12	22uF x 8
	10uF x 6

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power SNB 45W : 94A

Spec	Real
470uF/4mohm x 4	470uF/4mohm x 3
22uF x 16	22uF x 14
10uF x 10	10uF x 9

CPU VCCPL SNB 45W : 1.5A

Spec	Real
330uF/7mohm x 1	10uF x 1
10uF x 1	1uF x 2
1uF x 2	

CPU MCH SNB 45W : 5A

Spec	Real
330uF/6mohm x 1	10uF x 8
10uF x 6	

CPU MCH SNB 45W : 6A

Spec	Real
330uF/6mohm x 1	10uF x 3
10uF x 3	

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

Ra	EV@
	0 ohm

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to CPU

Place PU resistor close to CPU

CPU SA SNB 45W : 6A

Spec	Real
330uF/7mohm x 1	10uF x 3
10uF x 3	

DDR3 Standby Power Reduction

DDR3 Standby Power Reduction

Quanta Computer Inc.

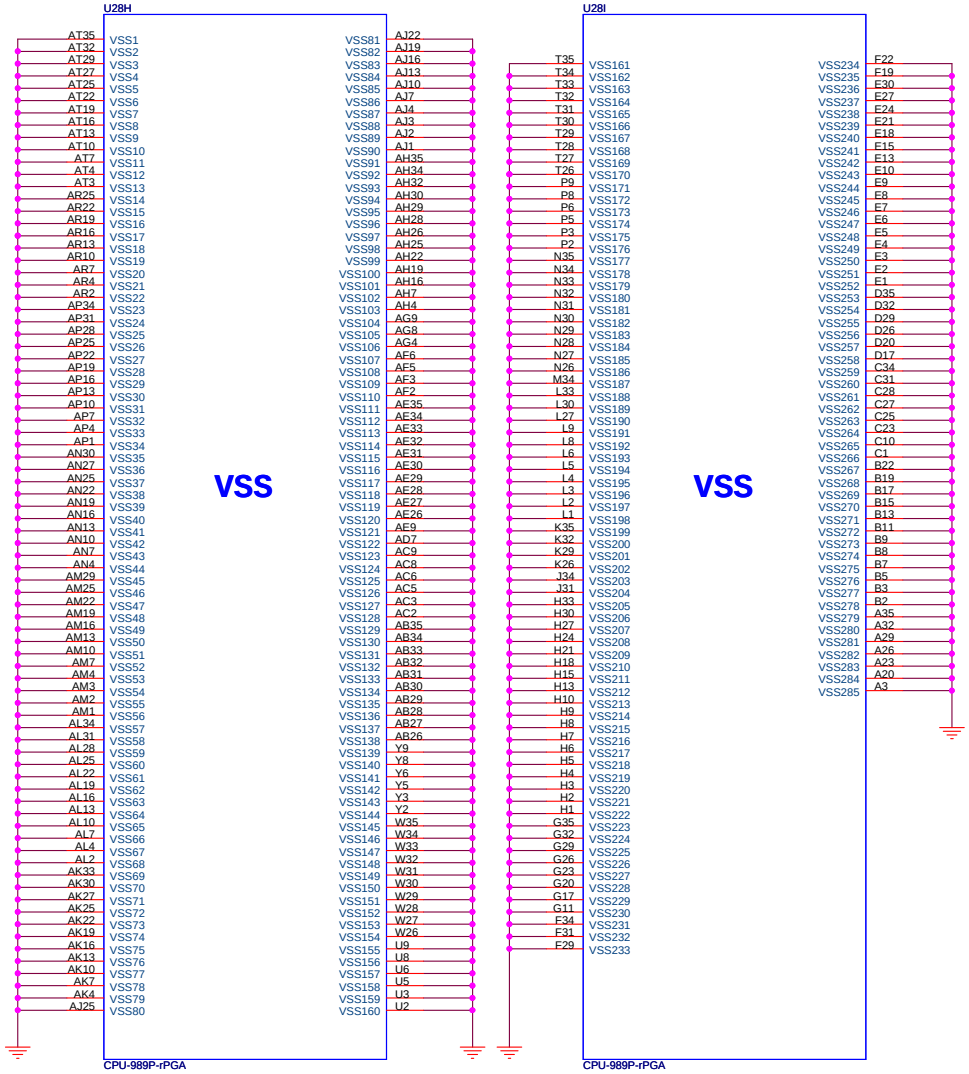
PROJECT : ZYG

Document Number: Sandy Bridge 3/4

Rev 1A

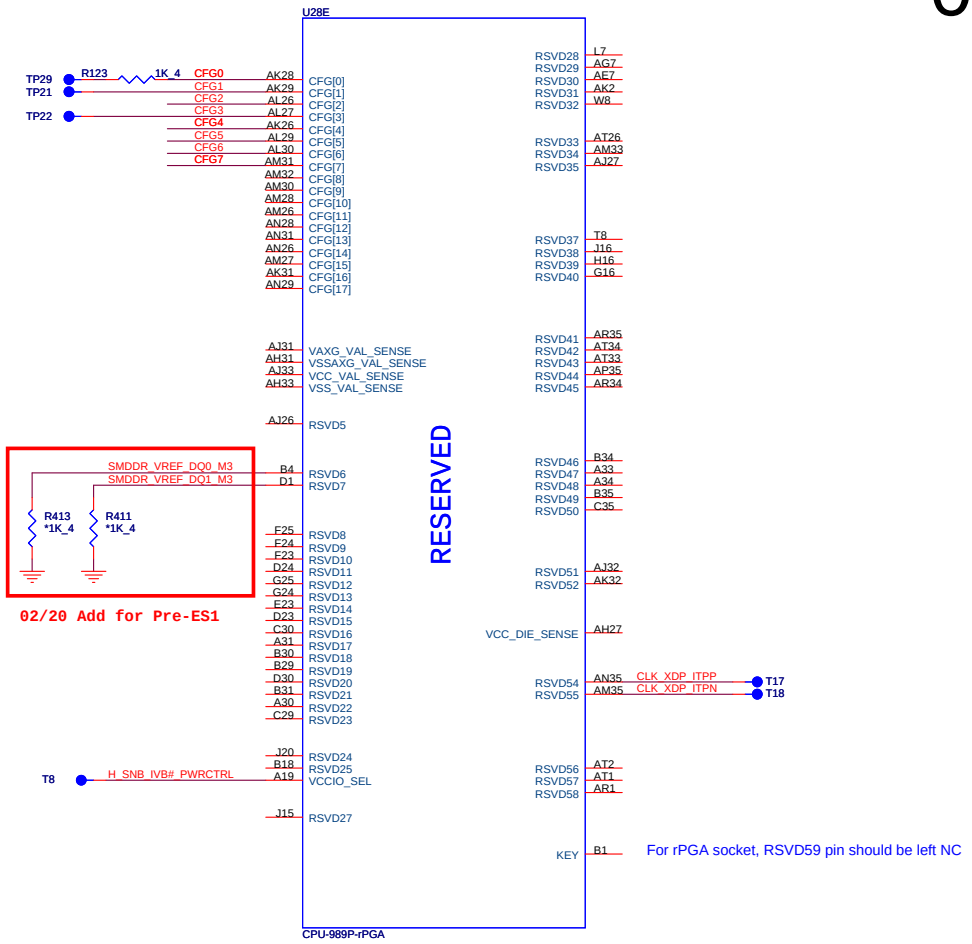
Date: Tuesday, February 22, 2011 Sheet 5 of 50

Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

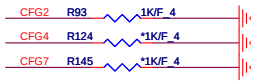
06

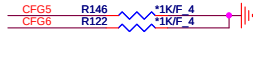


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





CFG[6:5] (PCIE Port Bifurcation Straps)

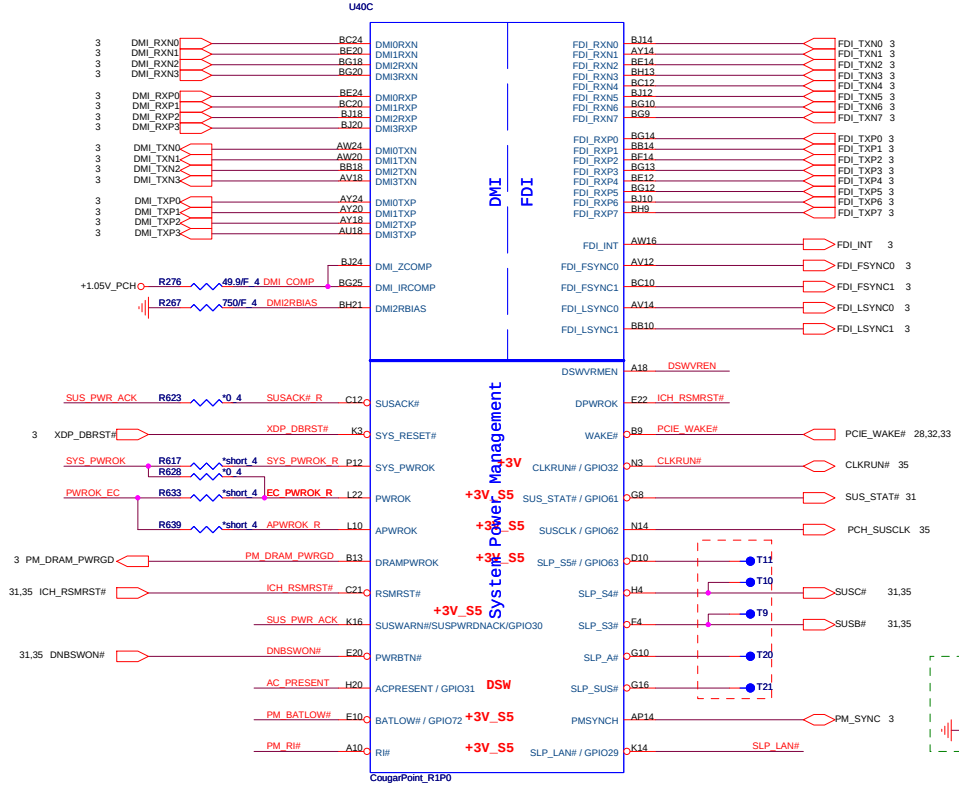
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT : ZYG

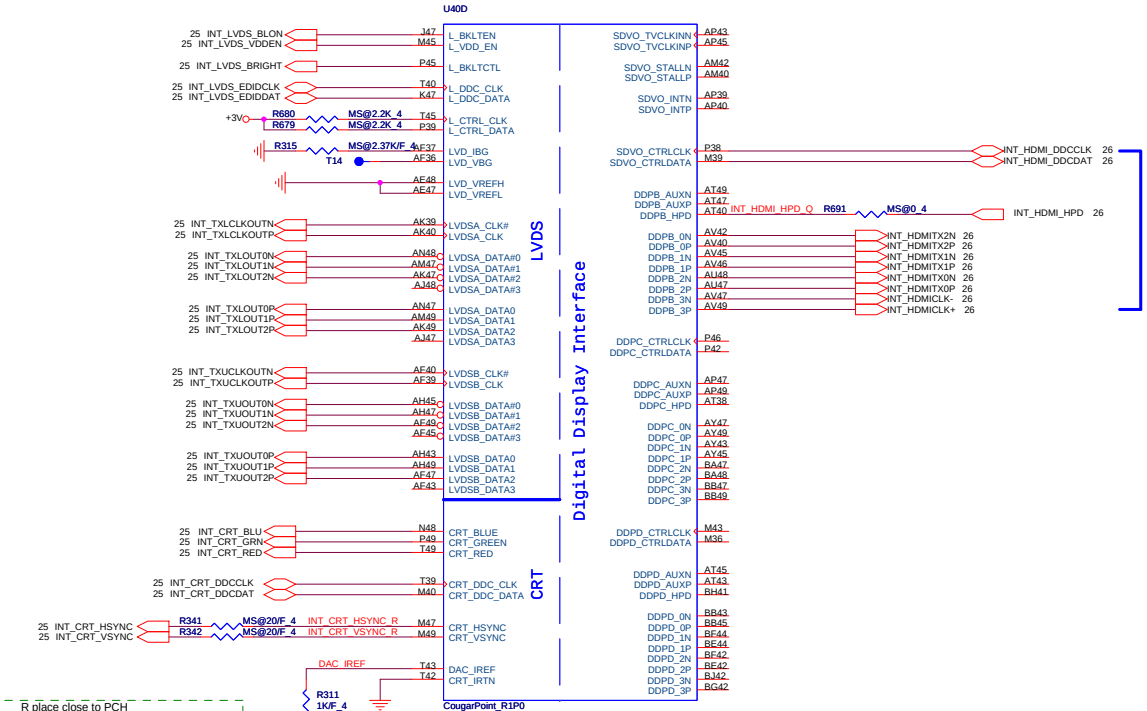
Size	Document Number	Rev
	Sandy Bridge 4/4	1A

Date: Monday, January 24, 2011 Sheet 6 of 50

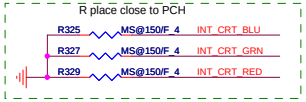
Cougar Point (DMI,FDI,PM)



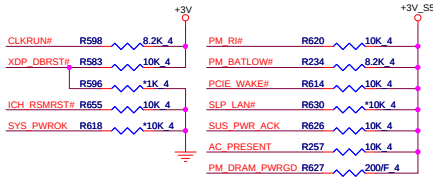
Cougar Point (LVDS,DDI)



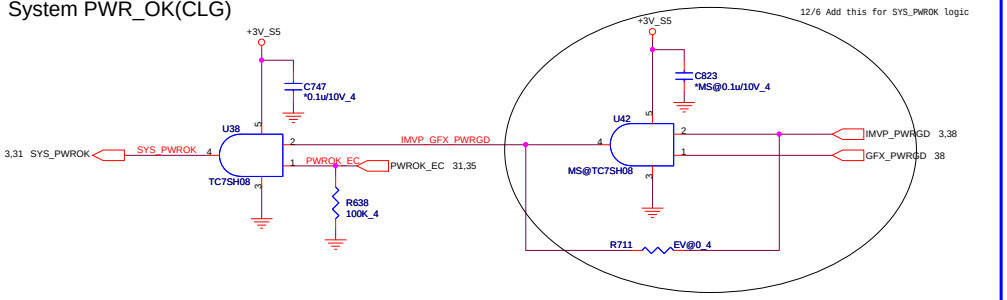
R place close to PCH

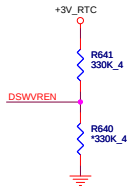


PCH Pull-high/low(CLG)



System PWR_OK(CLG)





On Die DSW VR Enable

High = Enable (Default)

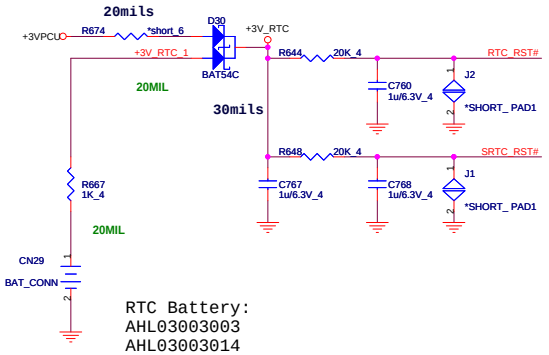
Low = Disable

Quanta Computer Inc.

PROJECT : ZYG

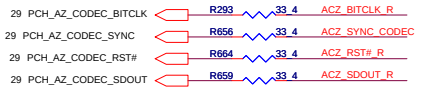
Size	Document Number	Rev
	Cougar Point 1/6	1A
Date: Tuesday, February 22, 2011	Sheet 7 of 50	

RTC Circuitry(RTC)



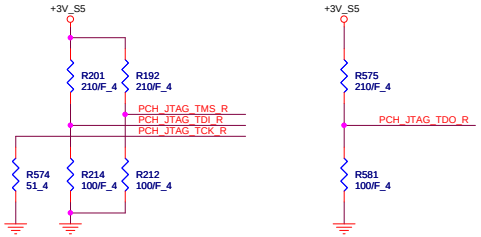
RTC Battery:
AHL03003003
AHL03003014
AHL030M0009

HDA Bus(CLG)

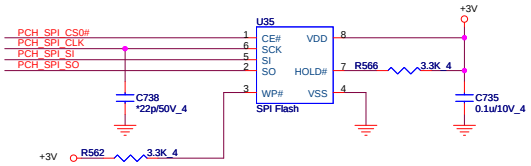


PCH JTAG Debug (CLG)

if no used PCH XDP, please reserved for S5 leakage

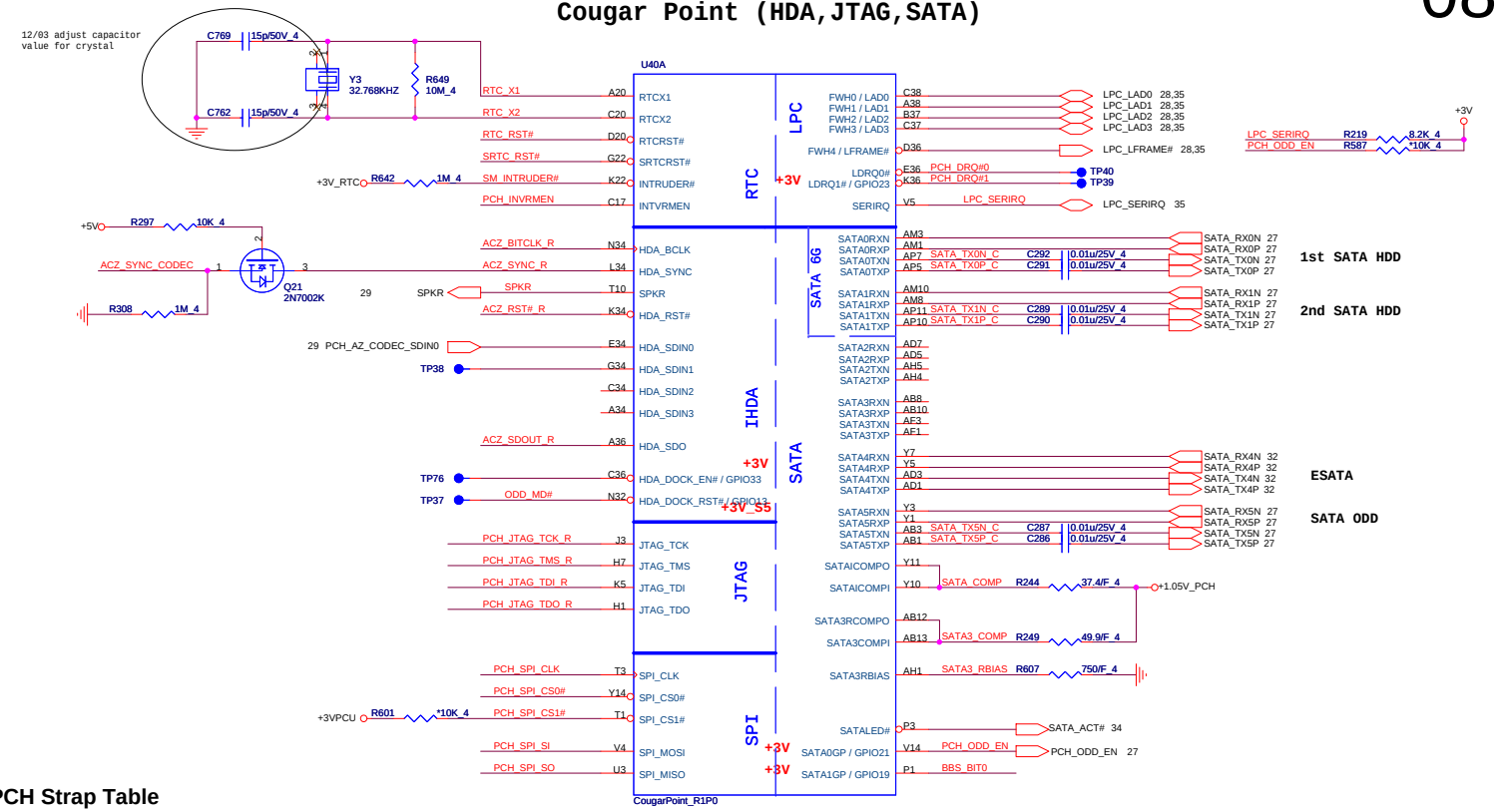


PCH Dual SPI (CLG)



PCH2(CLG)

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R198 *1K_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R672 *1K_4 PCI_GNT3# 9
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R643 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC	R673 *1K_4 BBS_BIT1 9 R600 *1K_4 BBS_BIT0
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K) 35	ME_WR# R660 *short_4 ACZ_SDOUT_R
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R606 2.2K_4 +1.8V R608 *1K_4 DF_TVS 10 H_SNB_IVB# 3
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R625 *1K_4 PLL_ODVR_EN 10
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 R296 1K_4 ACZ_SYNC_R
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	Need check schematic
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)	

Quanta Computer Inc.
PROJECT : ZY6

Size	Document Number	Rev
	Cougar Point 2/6	1A

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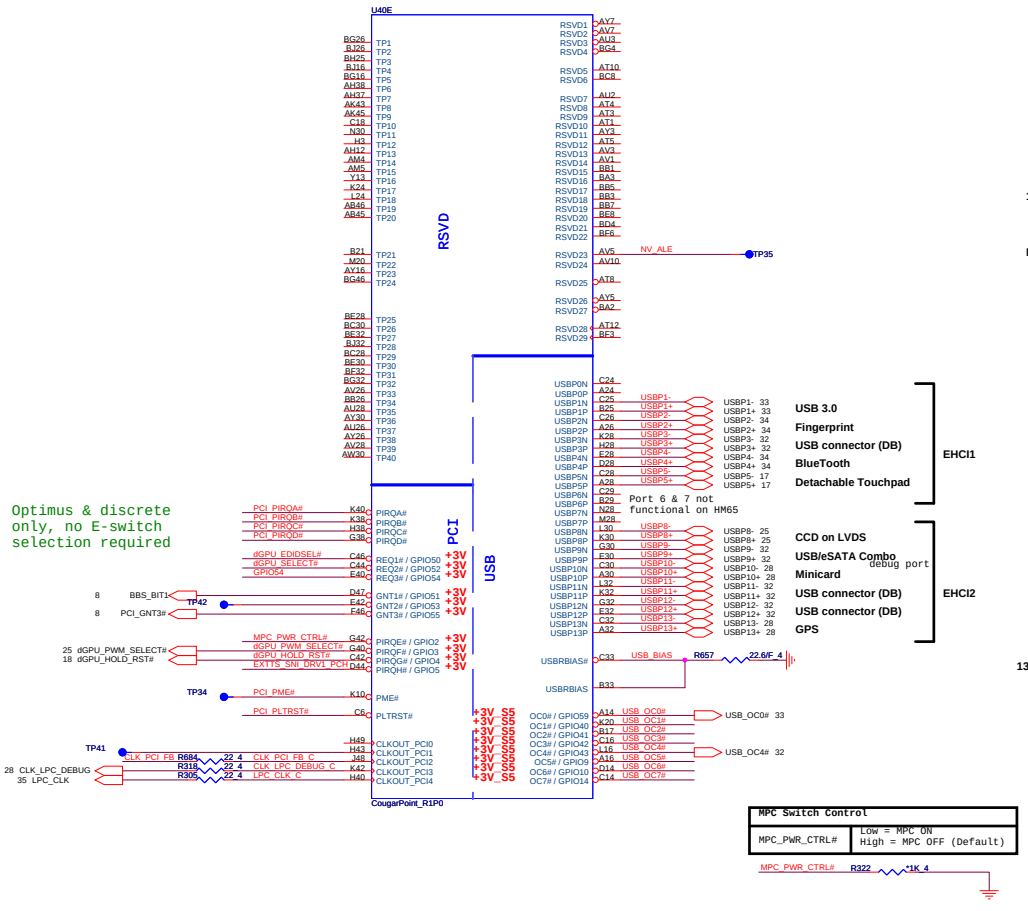
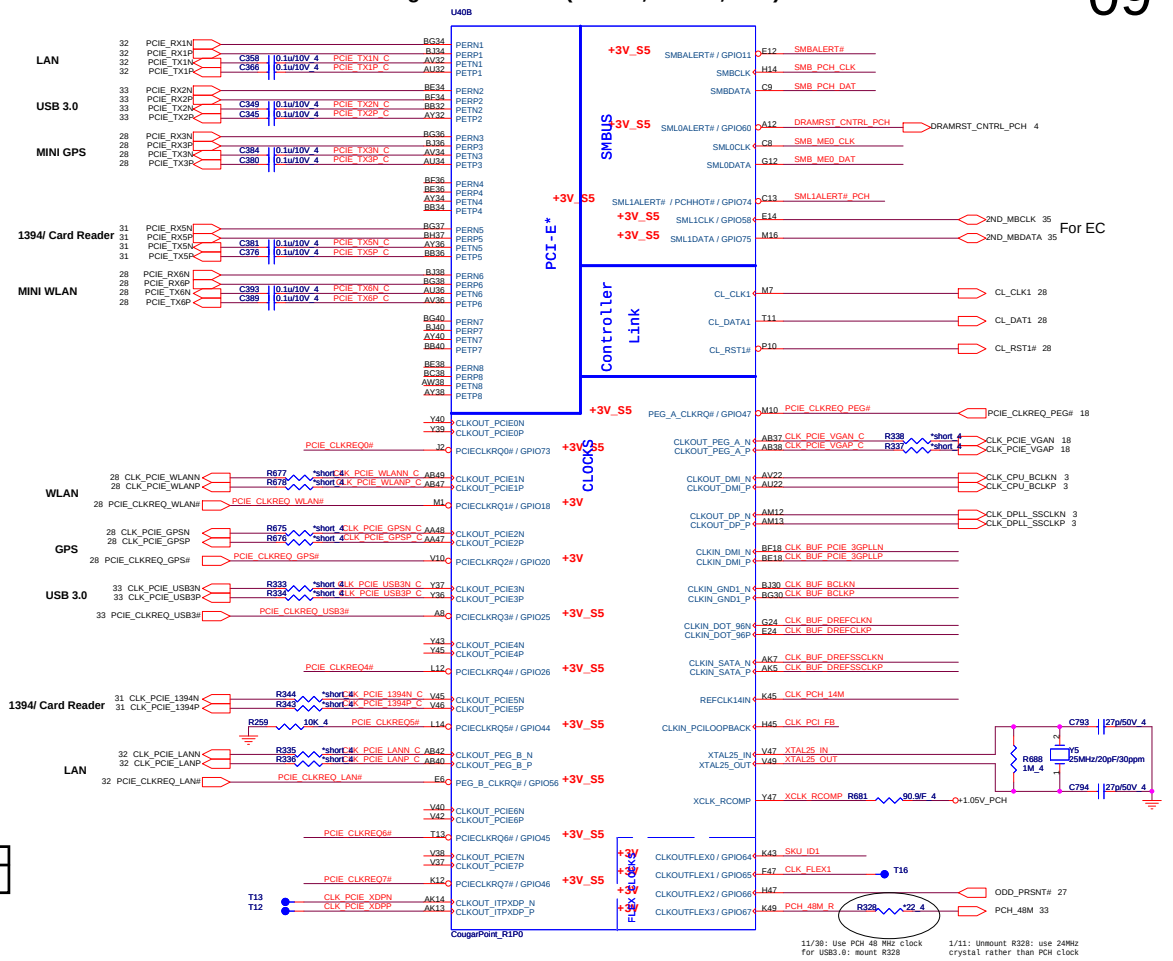
Cougar Point-M (PCI,USB,NVRAM)



MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

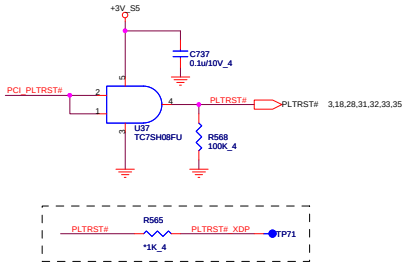
Cougar Point-M (PCI-E,SMBUS,CLK)



11/30: Use PCH 48 MHz clock for USB3.0: mount R328

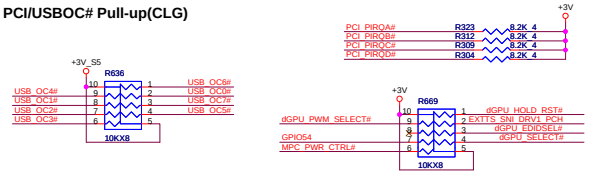
1/11: Unmount R328: use 24MHz crystal rather than PCH clock

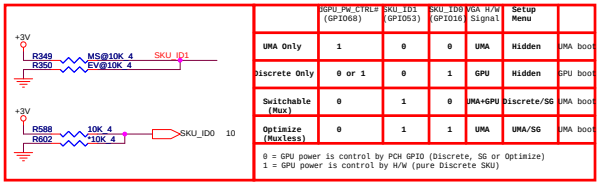
PLTRST#(CLG)



Placement 1K near AND Gate for XDP Function

PCI/USBOC# Pull-up(CLG)

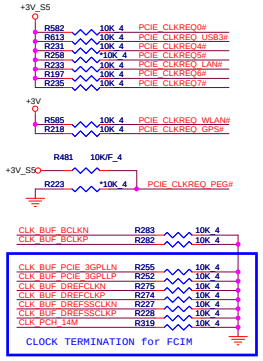




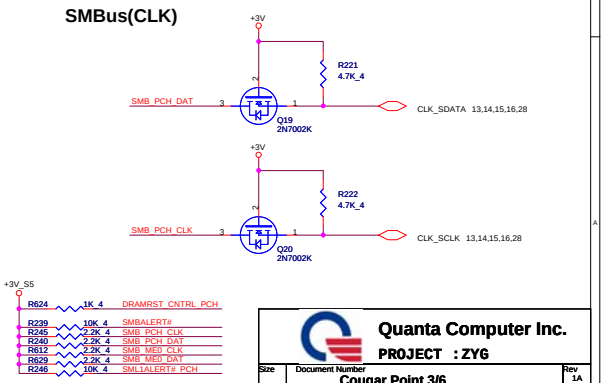
	DGPU_PW_CTRL# (GPIO68)	SKU_ID1 (GPIO53)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	Discrete/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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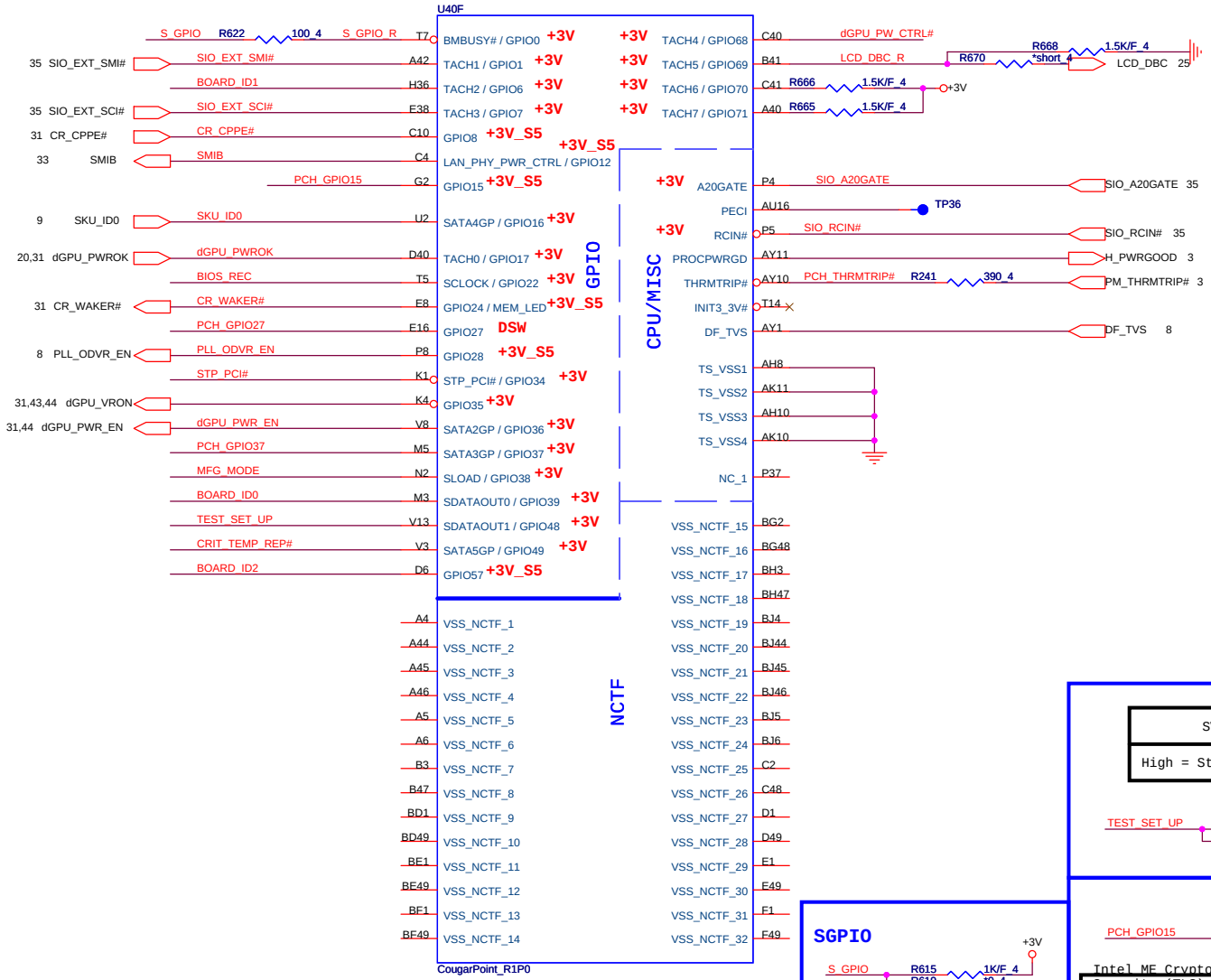
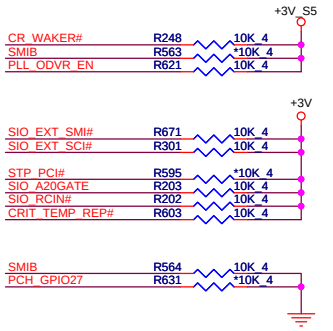
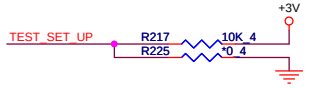
Cougar Point (GPIO,VSS_NCTF,RSVD)

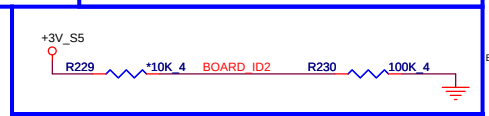


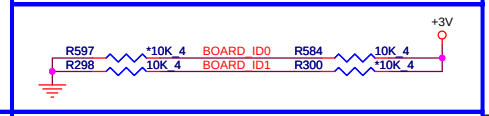
GPIO Pull-up/Pull-down(CLG)

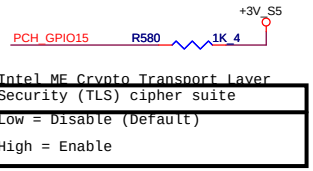


SV_SET_UP
High = Strong (Default)

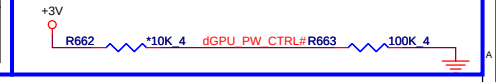




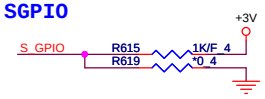


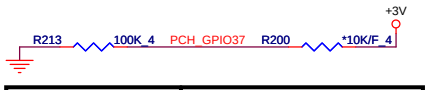


high	GPU power is control by H/W (pure Discrete SKU)
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

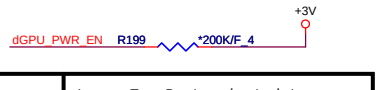


SGPIO

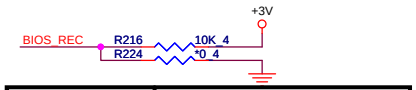




FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

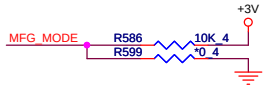


DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



BIOS RECOVERY	High = Disable (Default) Low = Enable

MFG-TEST



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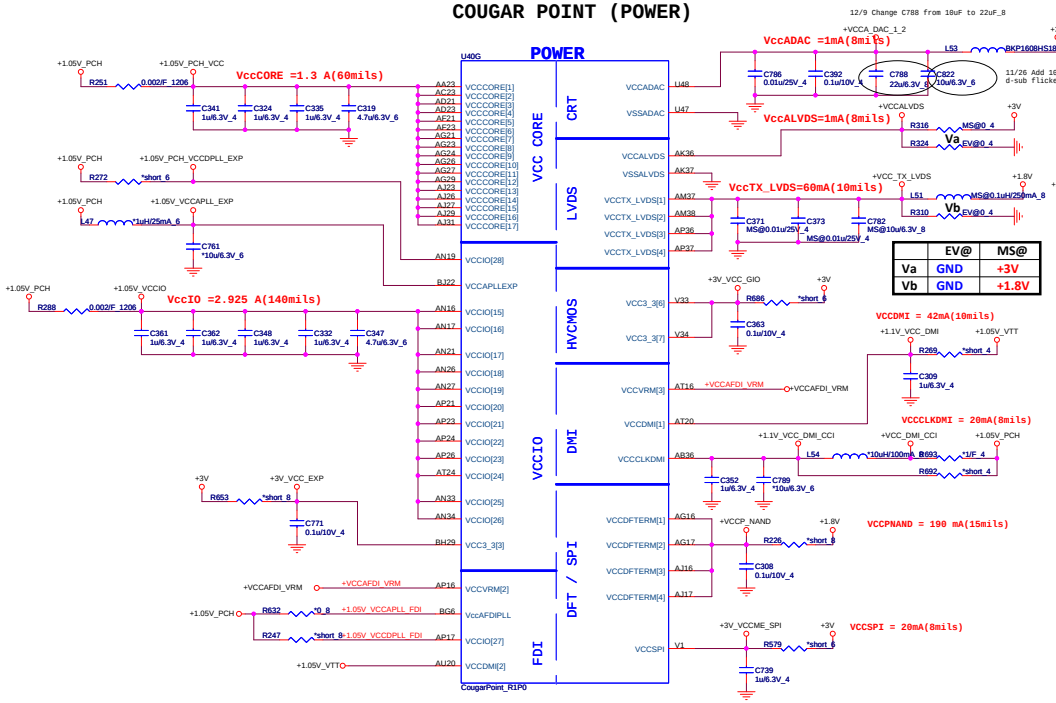
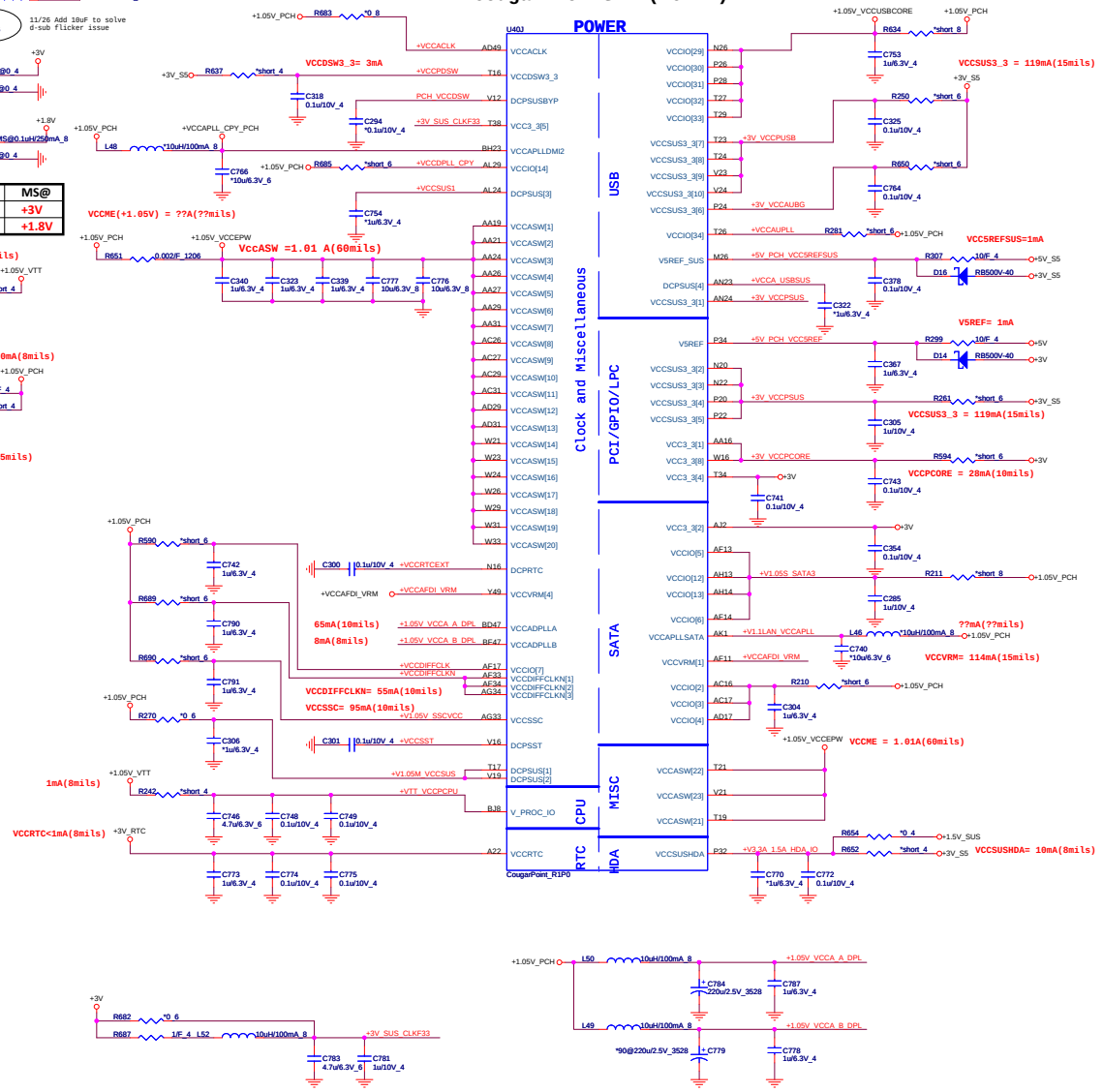
COUGAR POINT (POWER)



	EV@	MS@
Va	GND	+3V
Vb	GND	+1.8V

Cougar Point-M (POWER)



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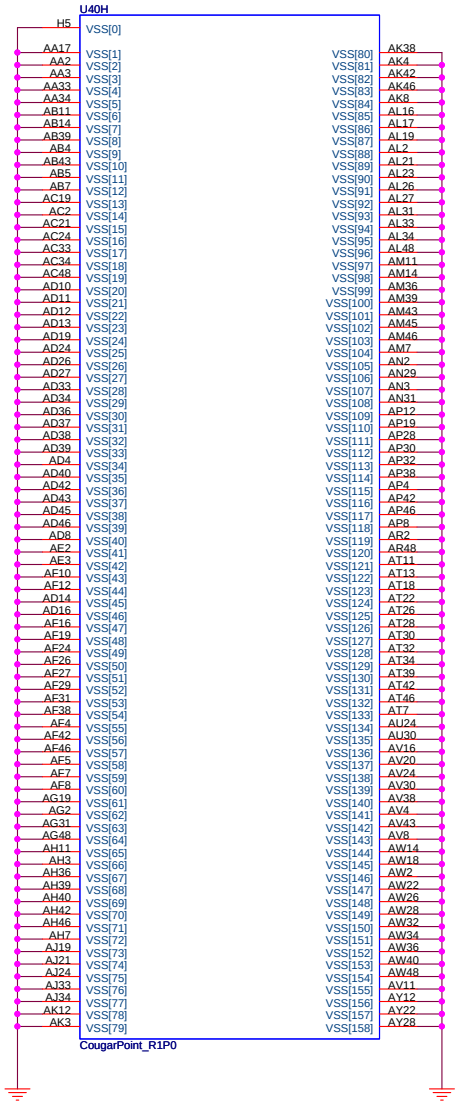
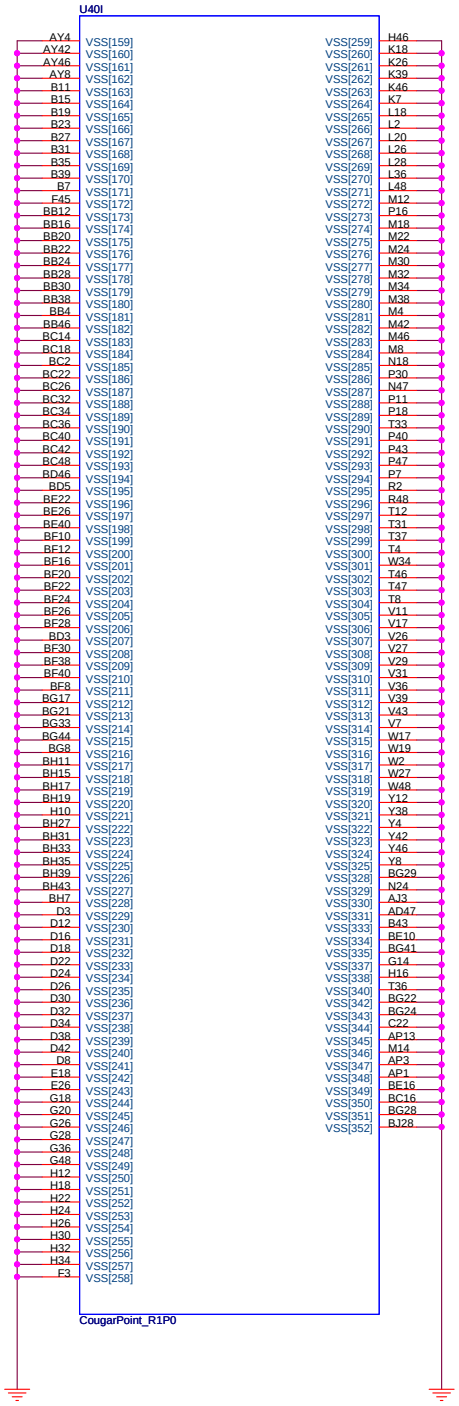
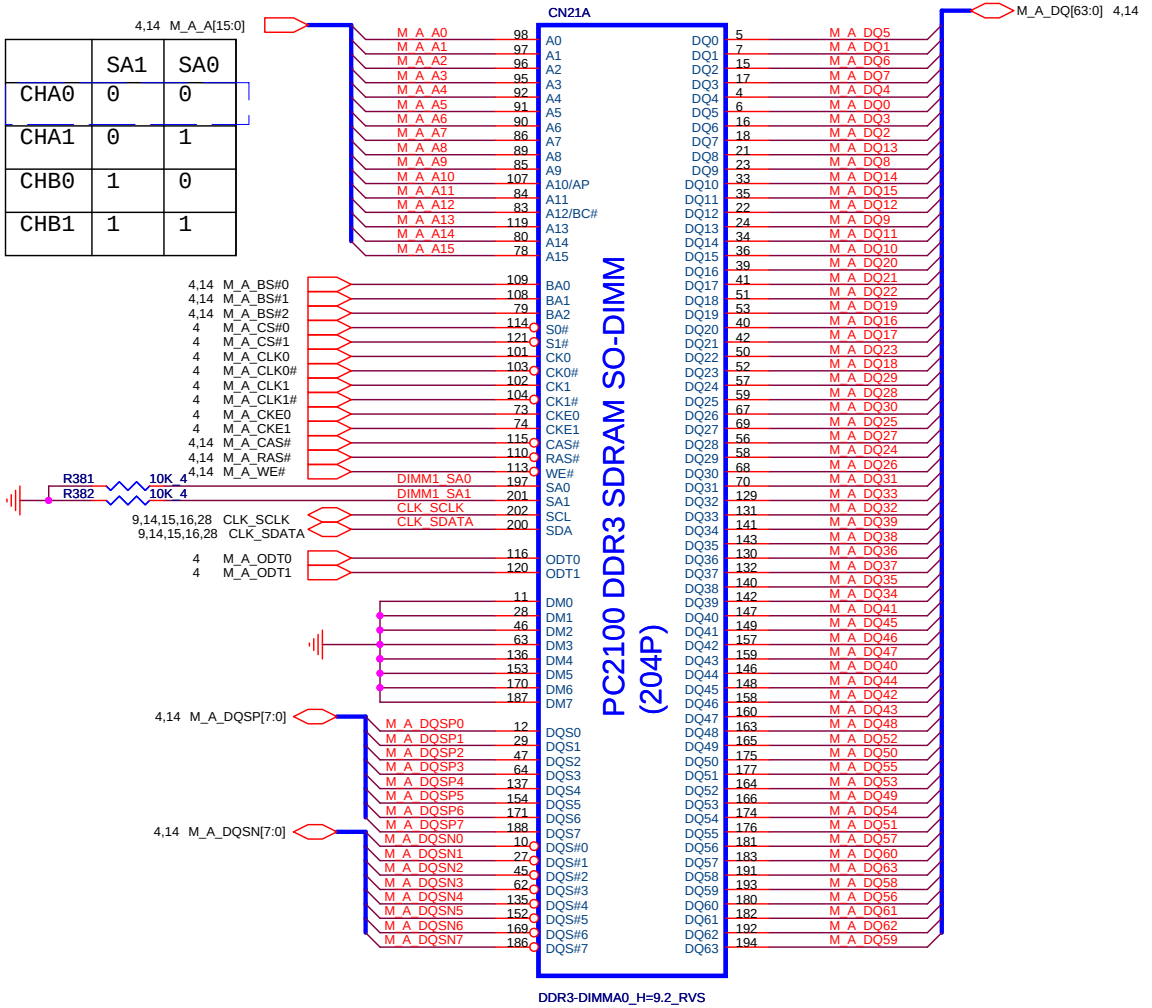
IBEX PEAK-M (GND)

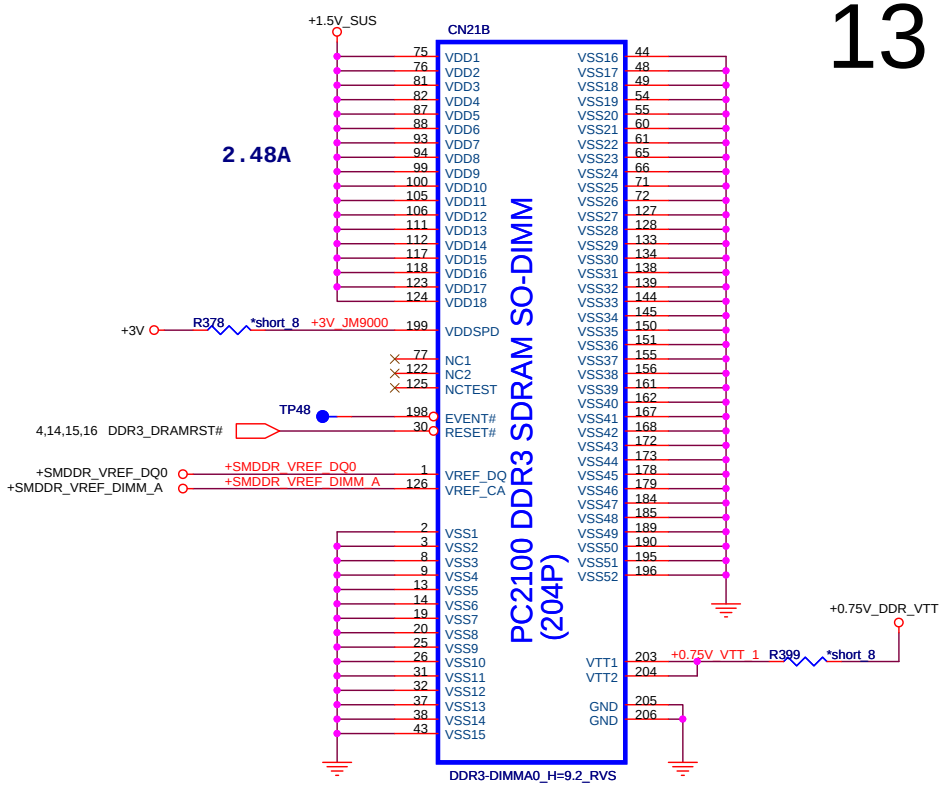


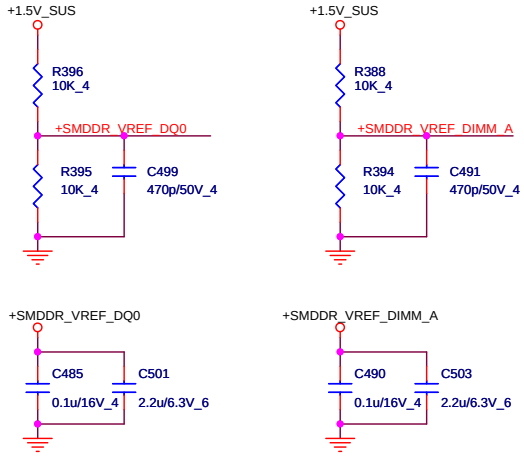


DDR3 DIMM-A0

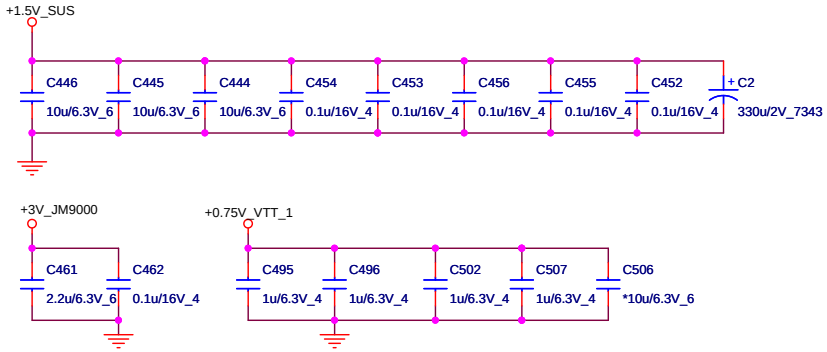
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1







Place these Caps near So-Dimm0.



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	DDRIII SO-DIMM-A0	1A

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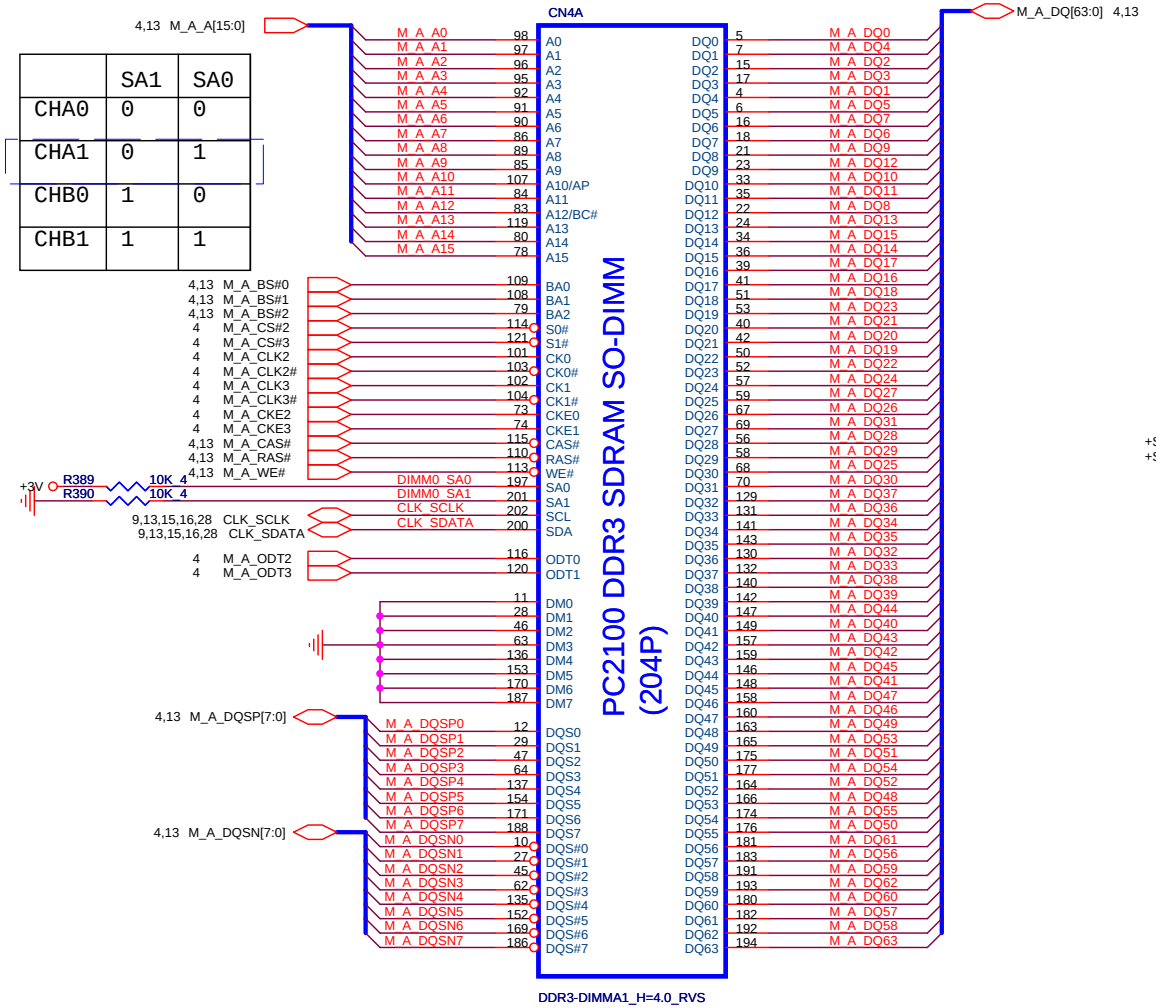
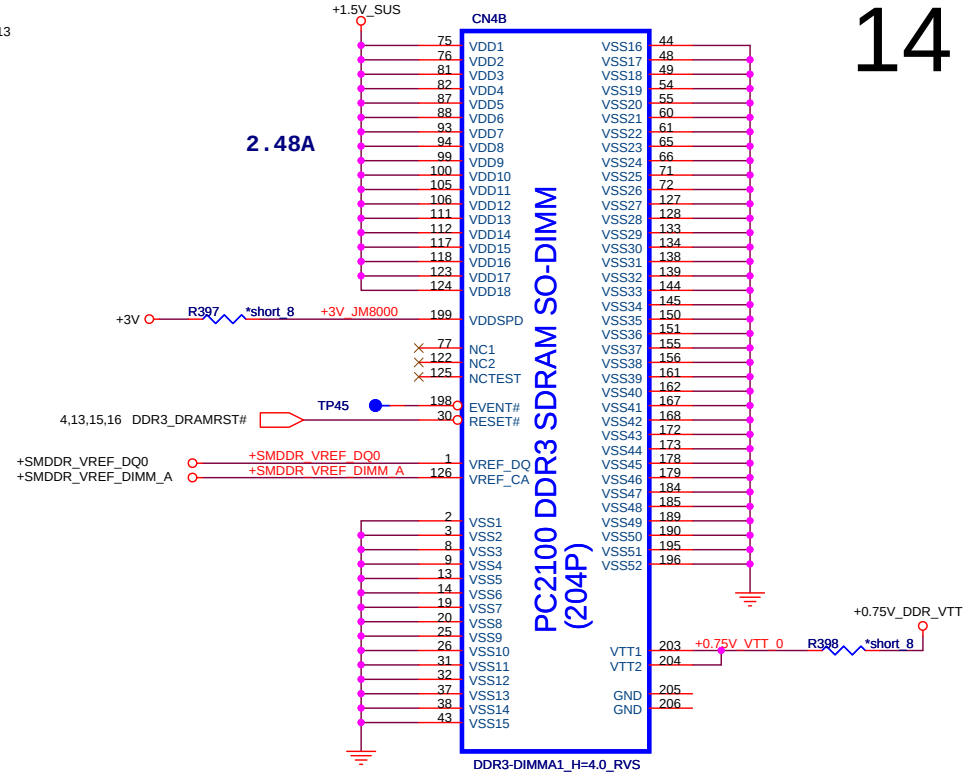
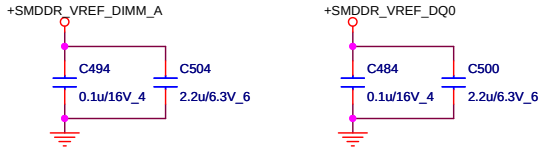
DDR3 DIMM-A1

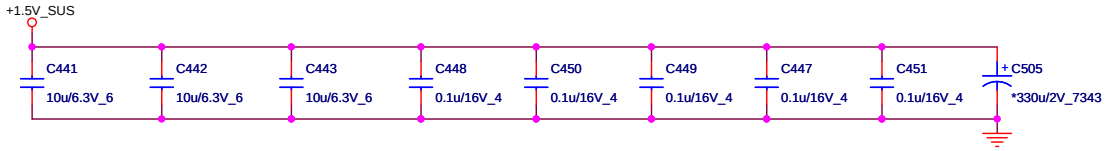
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

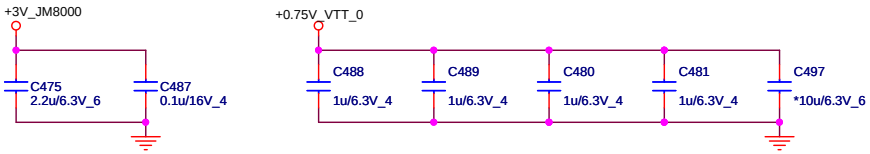






Place these Caps near So-Dimm0.





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	DDRIII SO-DIMM-A1	1A

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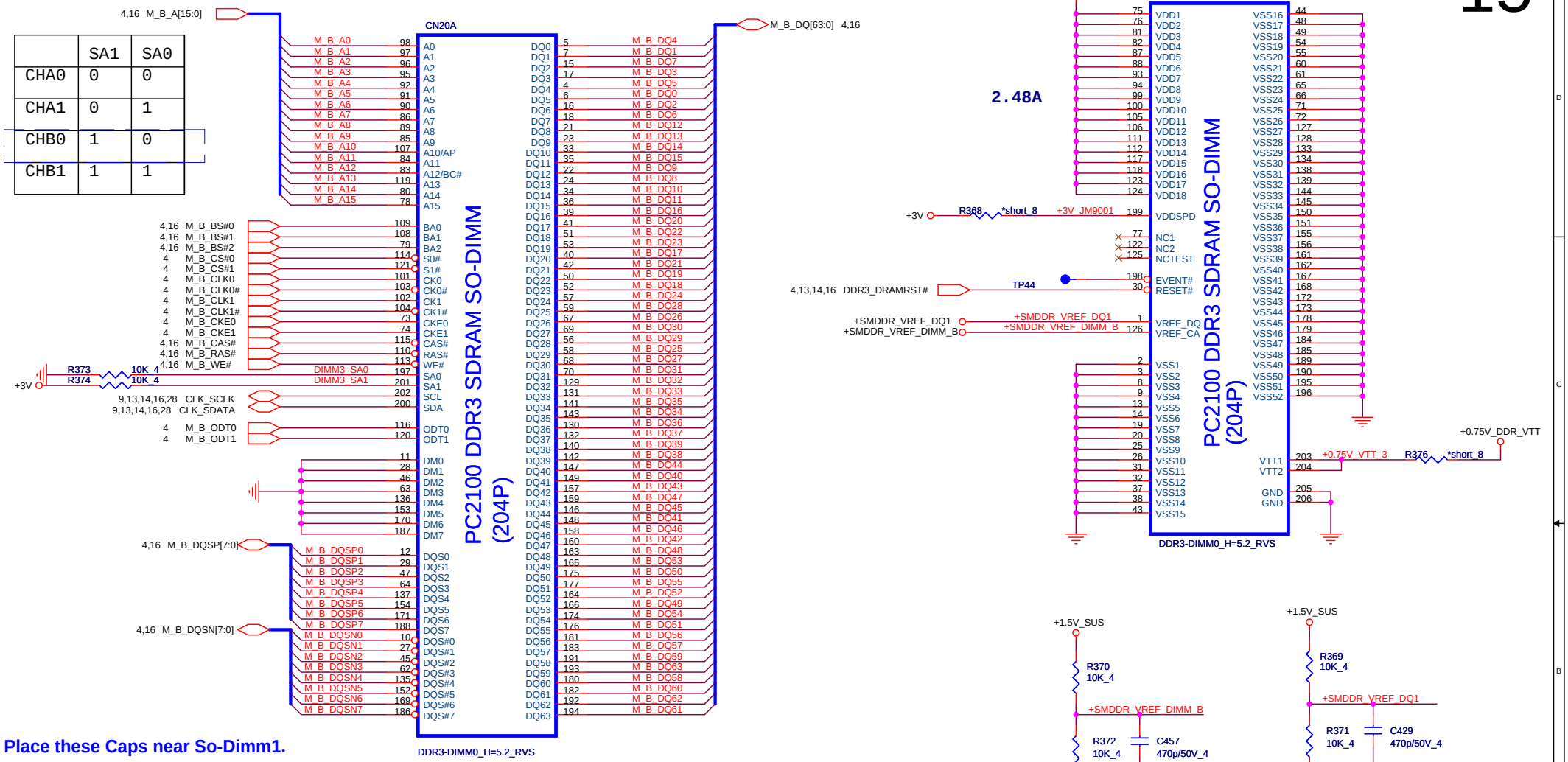
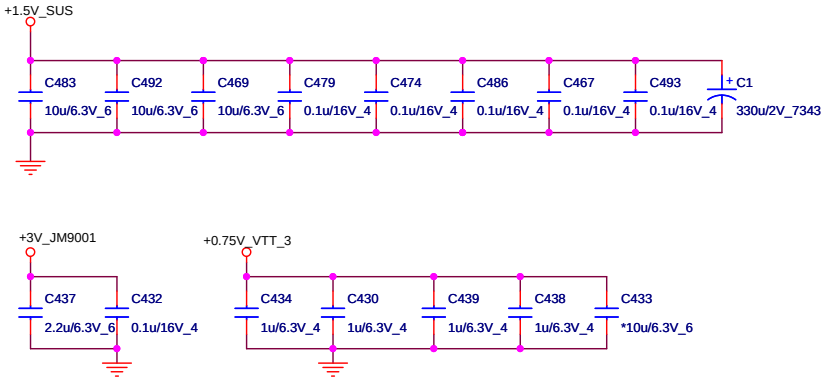
DDR3 DIMM-B0

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm1.



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	DDRIII SO-DIMM-B0	1A

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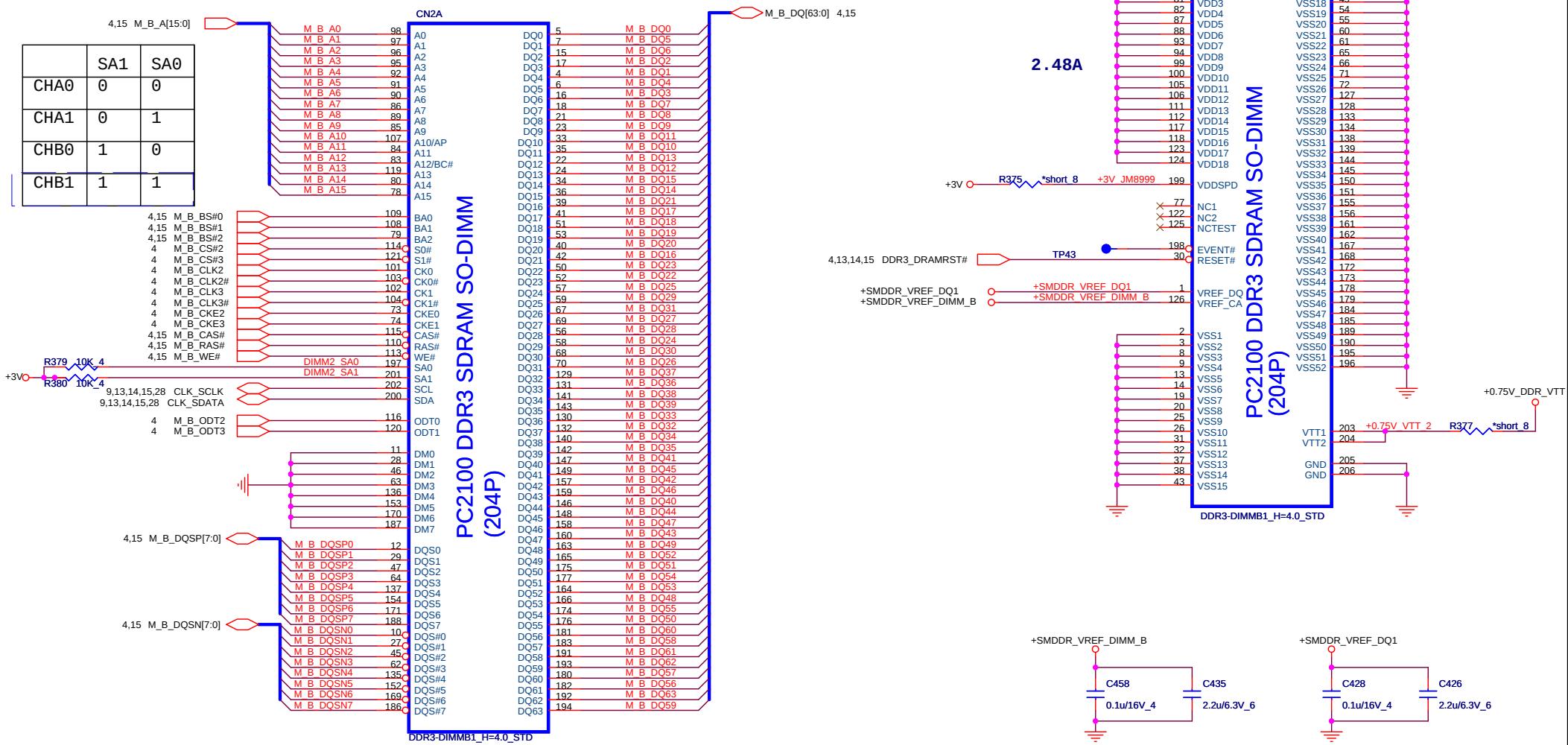
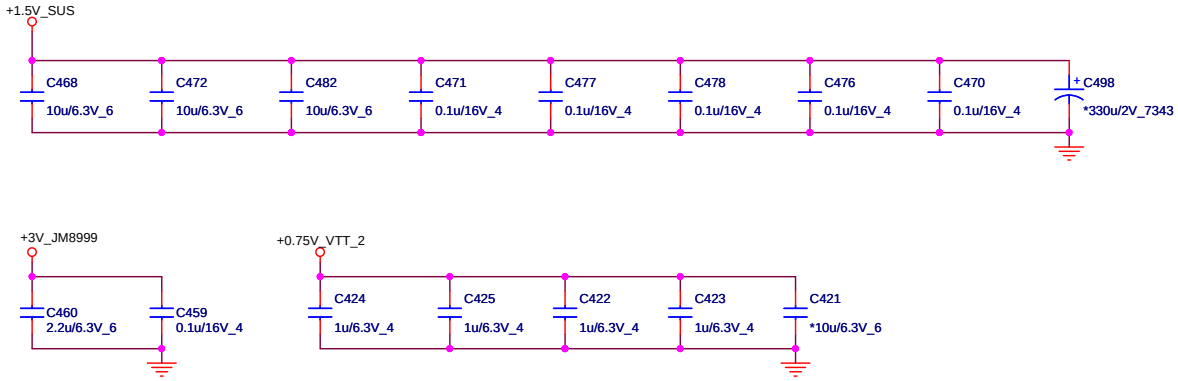
DDR3 DIMM-B1

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm1.



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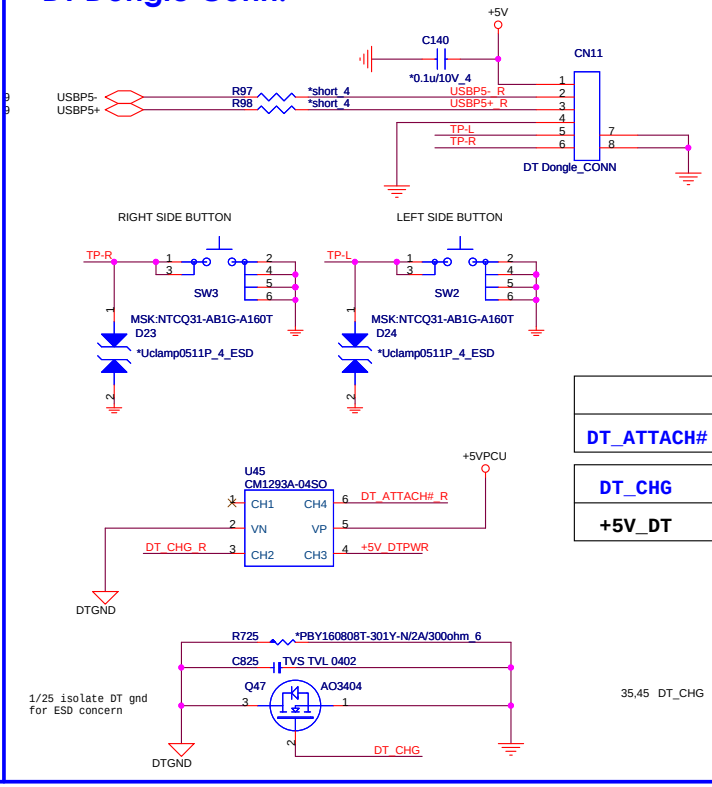
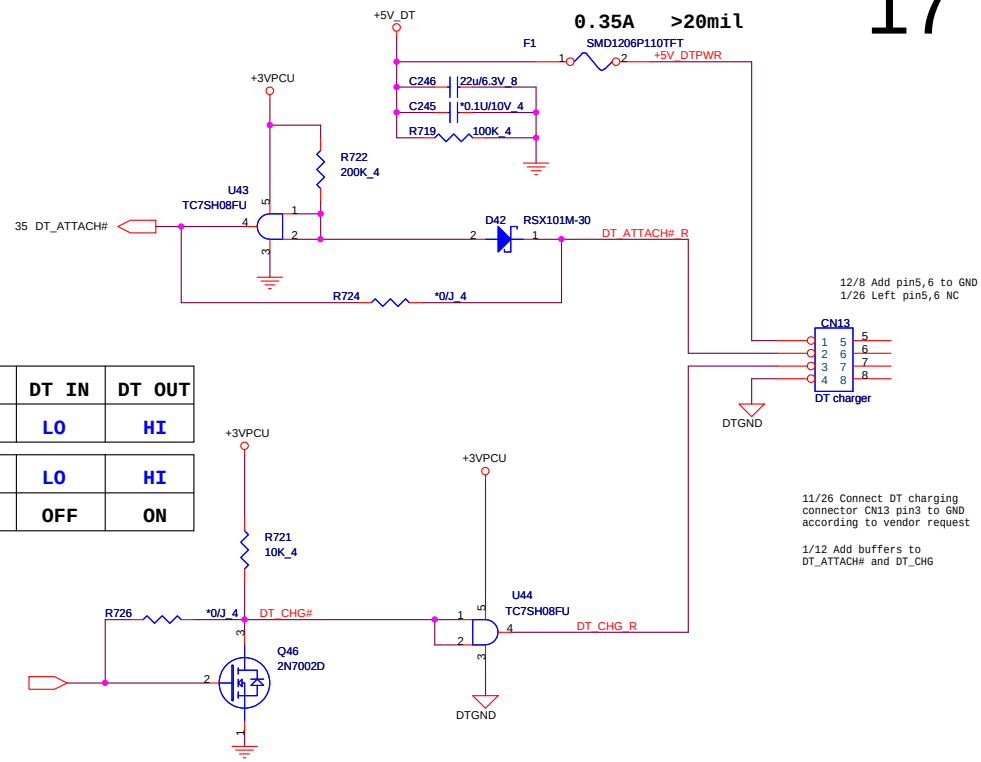
CPU XDP Connector(CPU)

XDP_PREQ#	CLK_PCIE_XDPN
XDP_PRDY#	XDP_DBRST#
XDP_BPM0	SMB_PCH_DAT
XDP_BPM1	SMB_PCH_CLK
XDP_BPM2	XDP_TDO
XDP_BPM3	XDP_TRST#
XDP_BPM4	XDP_TDI
XDP_BPM5	XDP_TMS
XDP_BPM6	XDP_TCLK
XDP_BPM7	SYS_PWROK
DNBSWON#	PCH_JTAG_TCK
CFG0----------1k	H_PWRGOOD----------1k
CLK_PCIE_XDPP	PLTRST#----------1k

DT Dongle Conn.

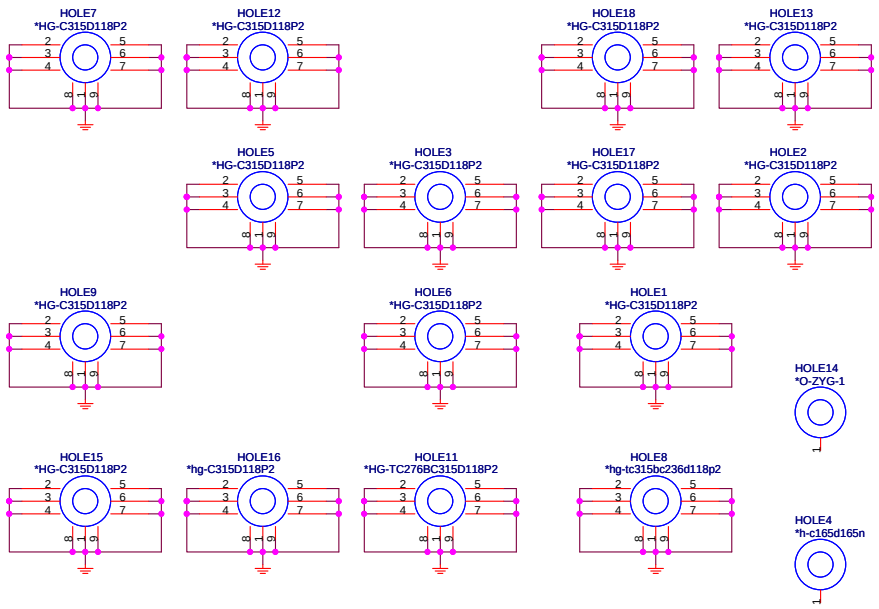


DT PW Conn.

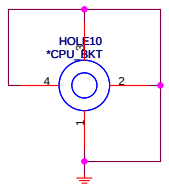


	DT IN	DT OUT
DT_ATTACH#	LO	HI
DT_CHG	LO	HI
+5V_DT	OFF	ON

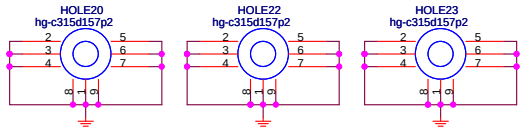
SCREW HOLE



BKT

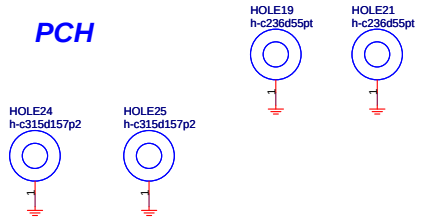


GPU

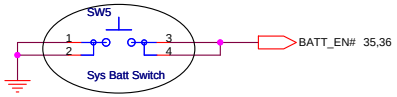


MiniCard

PCH



Battery Power Reset



12/8 Change to 4-pin

A-stage	SKU1	SKU2	SKU3	SKU4
GPU	N12E-GE	N12P-GS	N12P-GS	N12P-GS (dGPU)
VRAM	Hyinx 2G	Hynix 1G	Sam 2G	Hynix 2G

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	DT/ Batt. Rst ./ XDP/ Hole	1A

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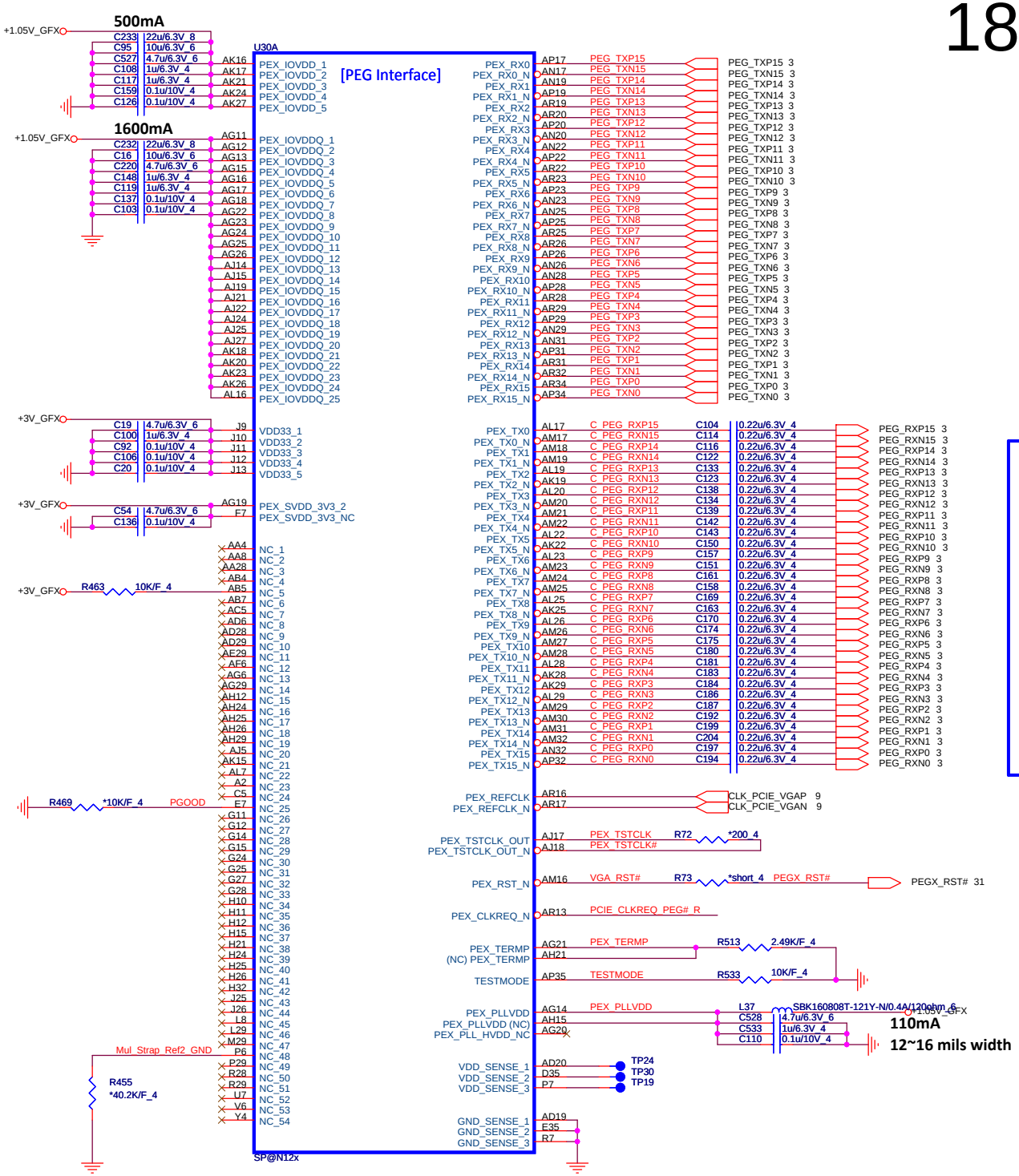

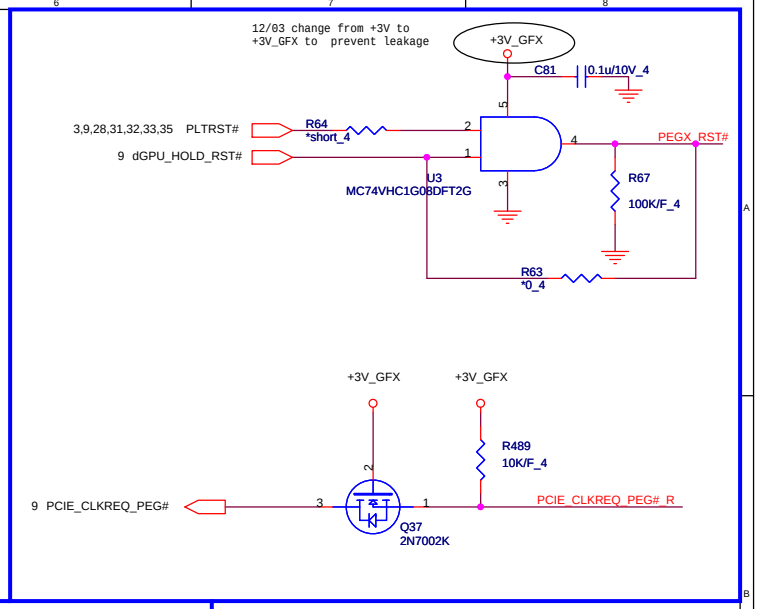

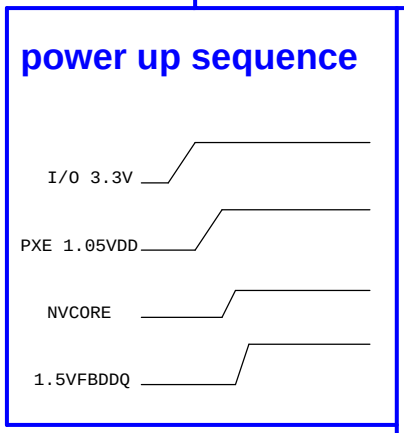

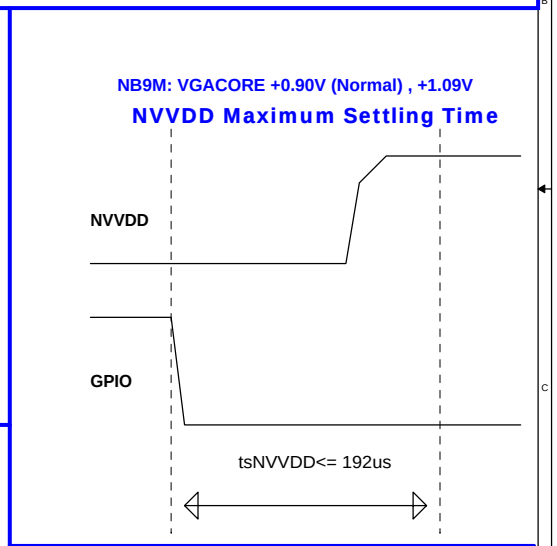

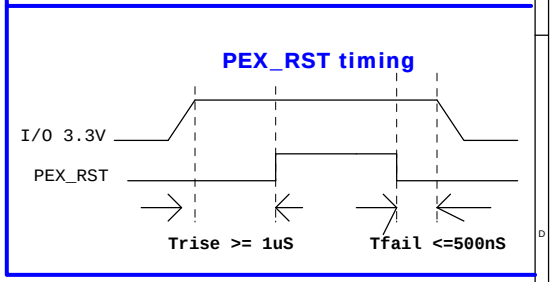

PEX_PLLVDD	GB2-128 / GB3-128 Under	Near
100nF ,10% X7R 0402	1	
1uF ,10% X7R 0603		1
4.7uF ,10% X5R 0603		1
120 Ohm 0603 ESR 180 mOhm		1

Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	DGPU 1/5 (PEG)	1A

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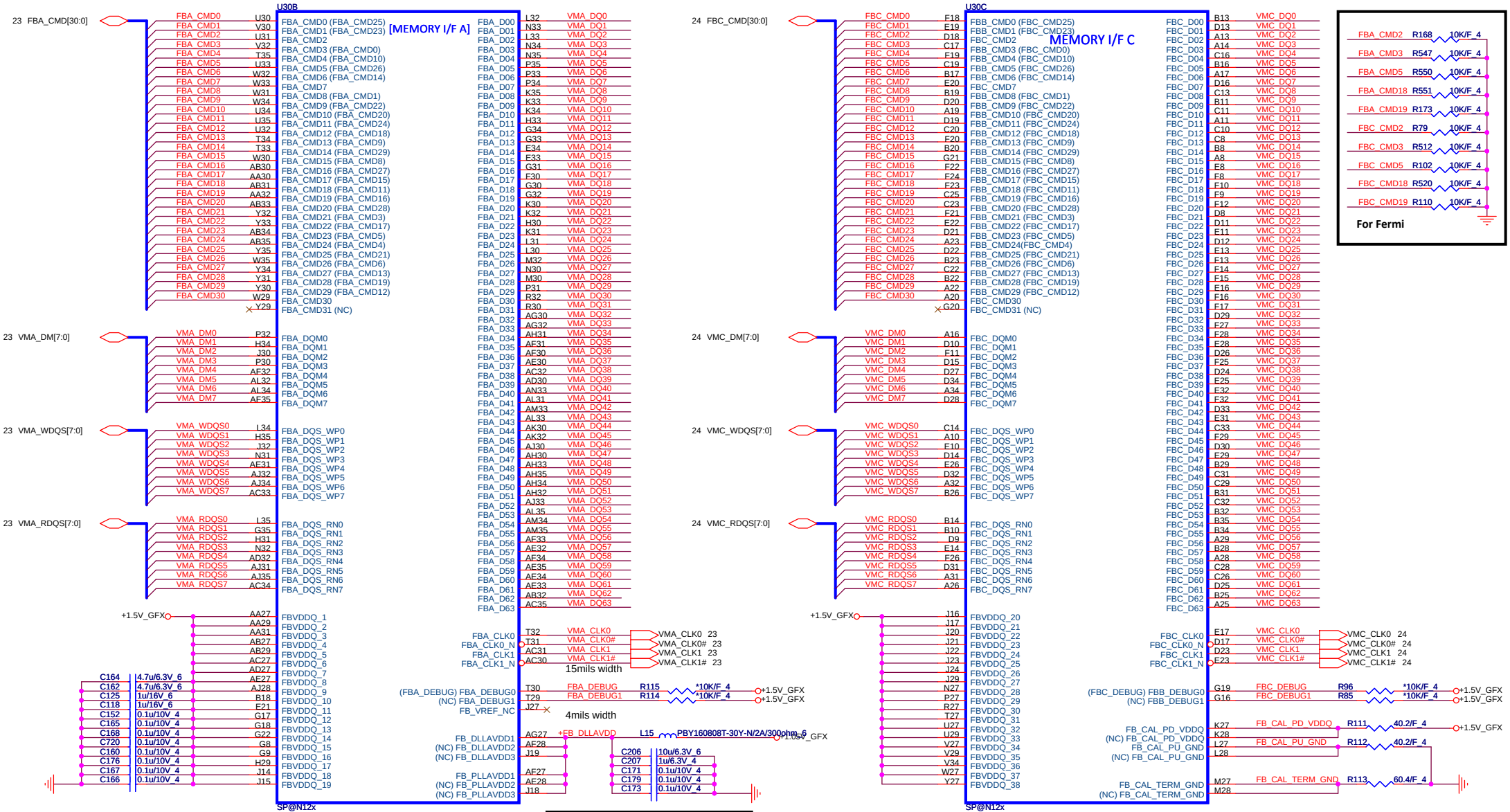


FBVDD	GB2-128 / GB3-128 Under	Near
0.1uF ,10% X7R 0603	8	
1uF ,10% X7R 0603		2
4.7uF ,10% X5R 0603		2

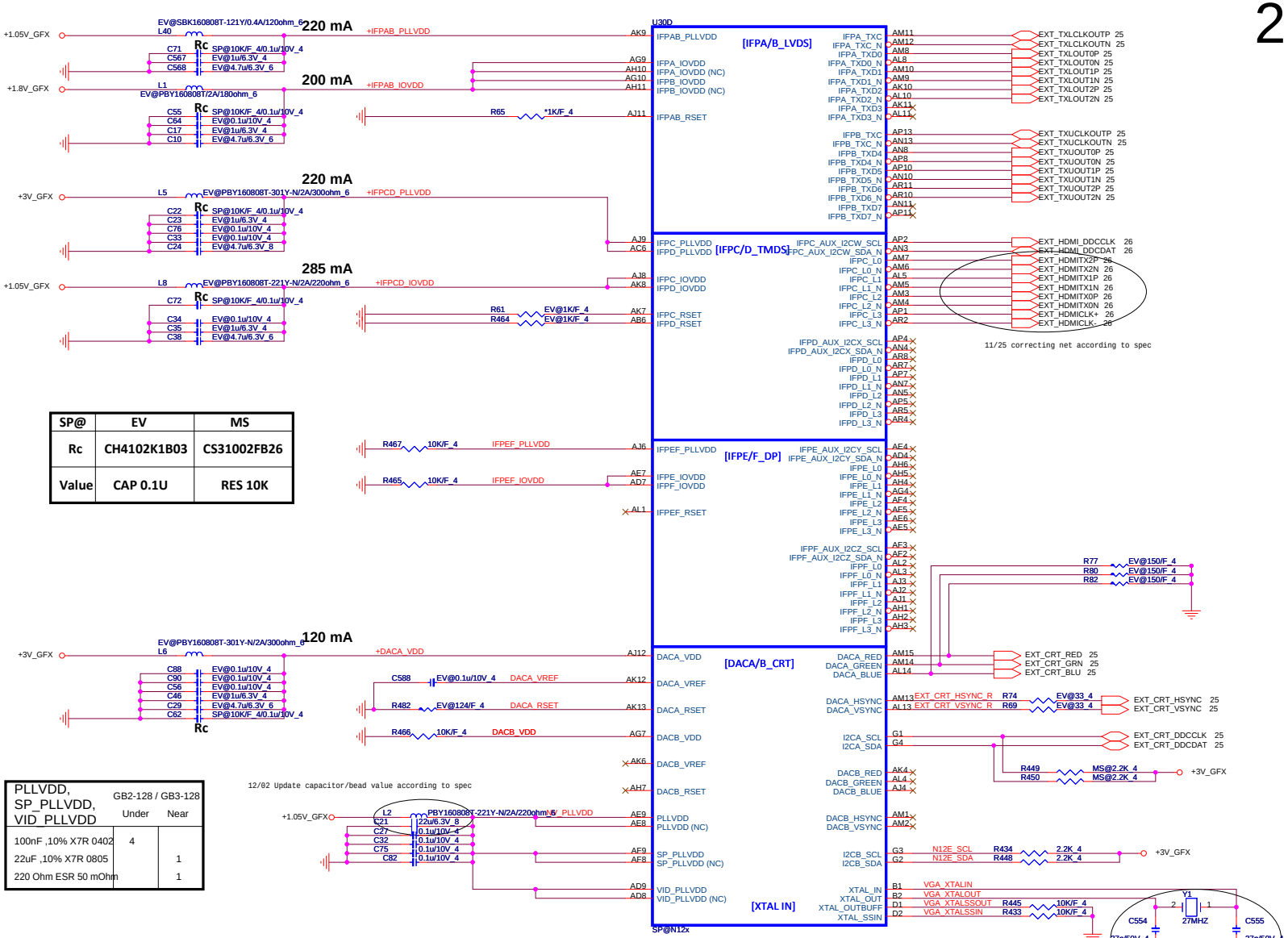
FB_DLLAVDD / FB_PLLAVDD	GB2-128 / GB3-128 Under	Near
100nF ,10% X7R 0402	3	
1uF ,10% X7R 0603		1
10uF ,10% X7R 0805		1
30 Ohm ESR 10 mOhm		1

Quanta Computer Inc.

PROJECT : ZYG

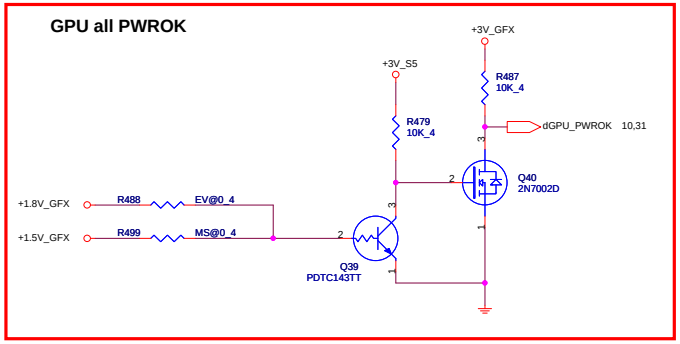
Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A

Date: Tuesday, February 22, 2011 Sheet 19 of 50



SP@	EV	MS
Rc	CH4102K1B03	CS31002FB26
Value	CAP 0.1U	RES 10K

PLLVDD, SP_PLLVDD, VID_PLLVDD	GB2-128 / GB3-128 Under	Near
100nF ,10% X7R 0402	4	
22uF ,10% X7R 0805		1
220 Ohm ESR 50 mOhm		1



IFPAB_PLLVDD	GB2-128 / GB3-128 Under	Near
100nF ,10% X7R 0402	1	
1uF ,10% X7R 0603		1
4.7uF ,10% X7R 0805		1
120 Ohm 0603 ESR 180 mOhm		1

DACx_VDD	GB2-128 / GB3-128 Under	Near
100nF ,10% X7R 0402	4	
1uF ,10% X5R 0402		1
4.7uF ,10% X5R 0805		1
300 Ohm 0603 ESR 250 mOhm		1

IFPC/D/E_ PLLVDD	GB2-128 / GB3-128 Under	Near
100nF ,10% X7R 0402	3	
1uF ,10% X7R 0603		1
4.7uF ,10% X7R 0805		1
300 Ohm 0603 ESR 250 mOhm		1

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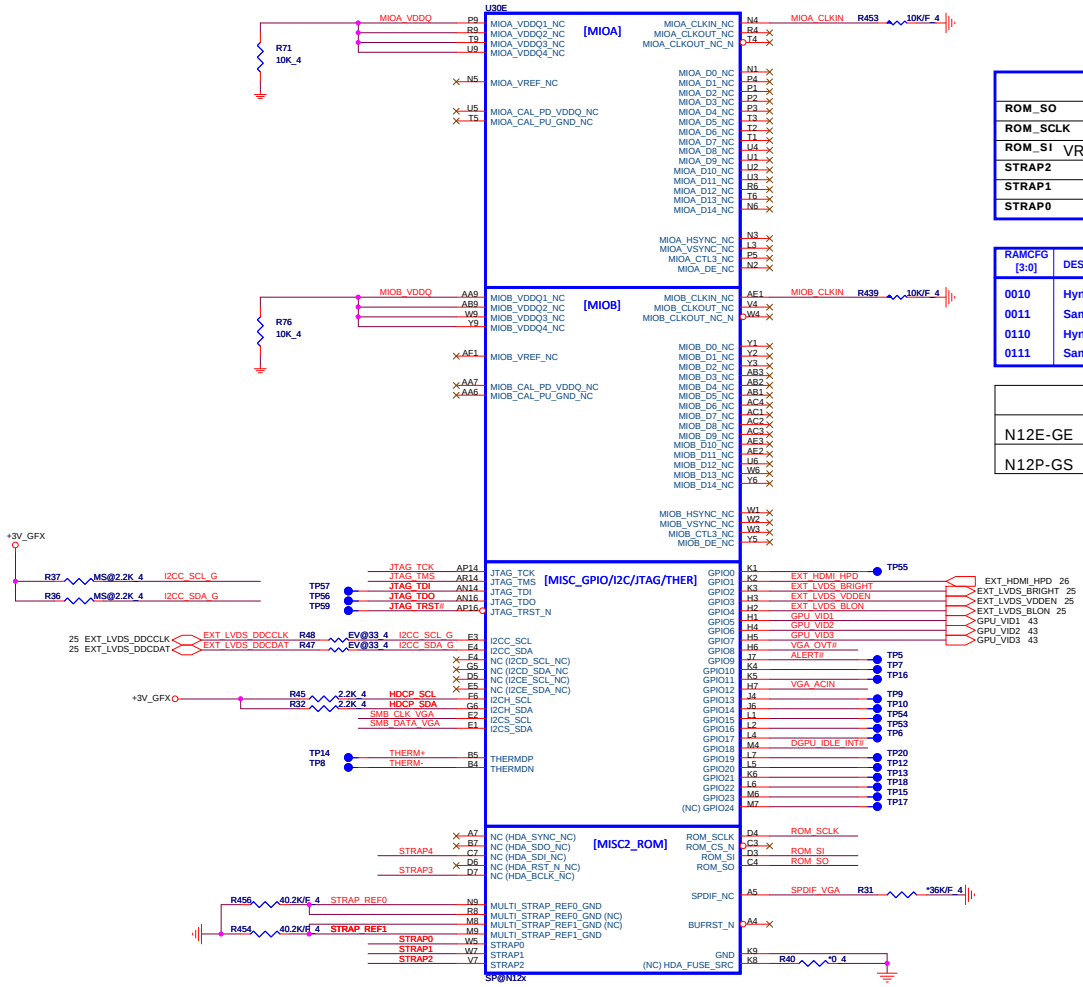
PROJECT : ZYG

Size	Document Number	Rev
	DGPU 3/5 (Display)	1A

Date: Tuesday, February 22, 2011 Sheet 20 of 50



	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12P-GS	N12P-GS	N12P-GS	N12P-GS	N12E-GE	N12E-GE	N12E-GE	N12E-GE
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001	0001	0001	0001	0001	0001	0001	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010	1010	1010	1010	0010	0010	0010	0010
ROM_SI VRAM	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010	0110	0011	0111	0010	0110	0011	0111
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100	0100	0100	0100	1110	1110	1110	1110
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	0110	0110	0110	0110	0110	0110	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111	1111	1111	1111	1111	1111	1111

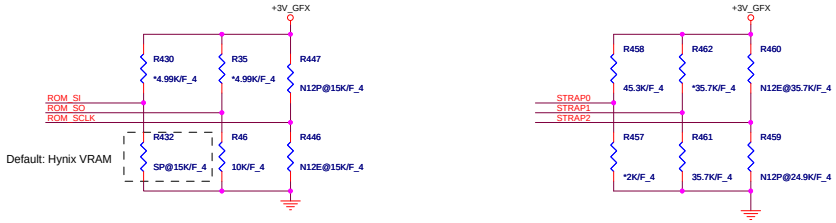
RAMCFG [3:0]	DESCRIPTION		Vendor P/N	ROM_SI	QCI	QCI B/S
0010	Hynix	DDR3 64Mx16x8, 1GB,900MHz	H5TQ1G63DFR-11C	PD 15K	AKD5LZWTW02	AKD5LZWTW05
0011	Samsung	DDR3 64Mx16x8, 1GB,900MHz	K4W1G1646G-BC11	PD 20K	AKD5EGGT500	AKD5EGGT503
0110	Hynix	DDR3 128Mx16x8, 2GB,900MHz	H5TQ2G63BFR-11C	PD 35K	AKD5MGWTW00	AKD5MGWTW03
0111	Samsung	DDR3 128Mx16x8, 2GB,900MHz	K4W2G1646C-HC11	PD 45K	AKD5MGWT500	AKD5MGWT503

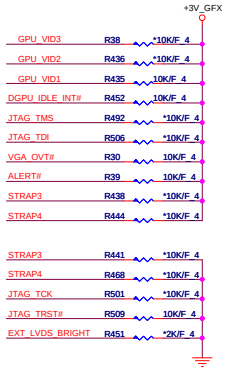
		QCI	B/S
N12E-GE	IC CTRL(1005P) N12E-GE-A1(BGA)	AJ0N12E0T00	AJ0N12E0T02
N12P-GS	IC CTRL(973P) N12P-GS-A1(BGA)	AJ0N12P0T04	AJ0N12P0T13

Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

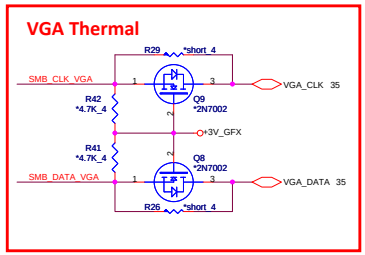
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

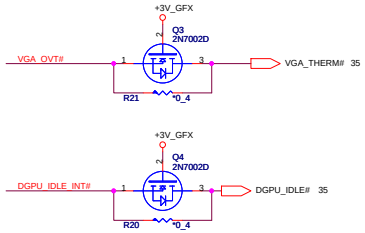


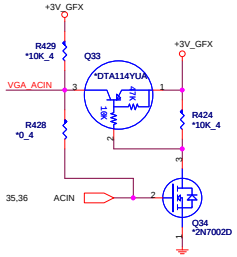


GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL





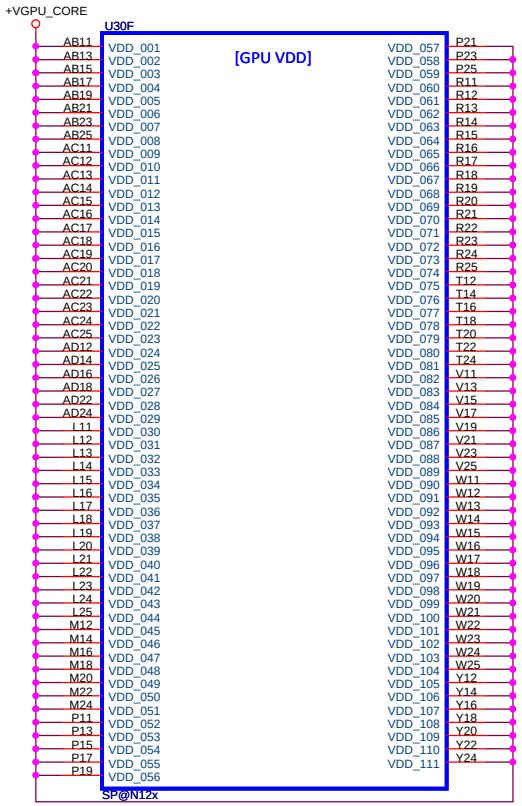


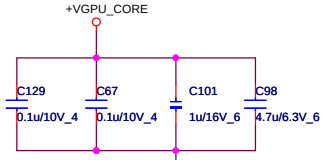
Quanta Computer Inc.

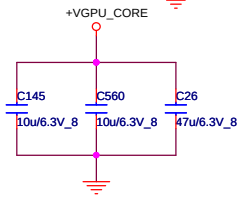
PROJECT : ZYG

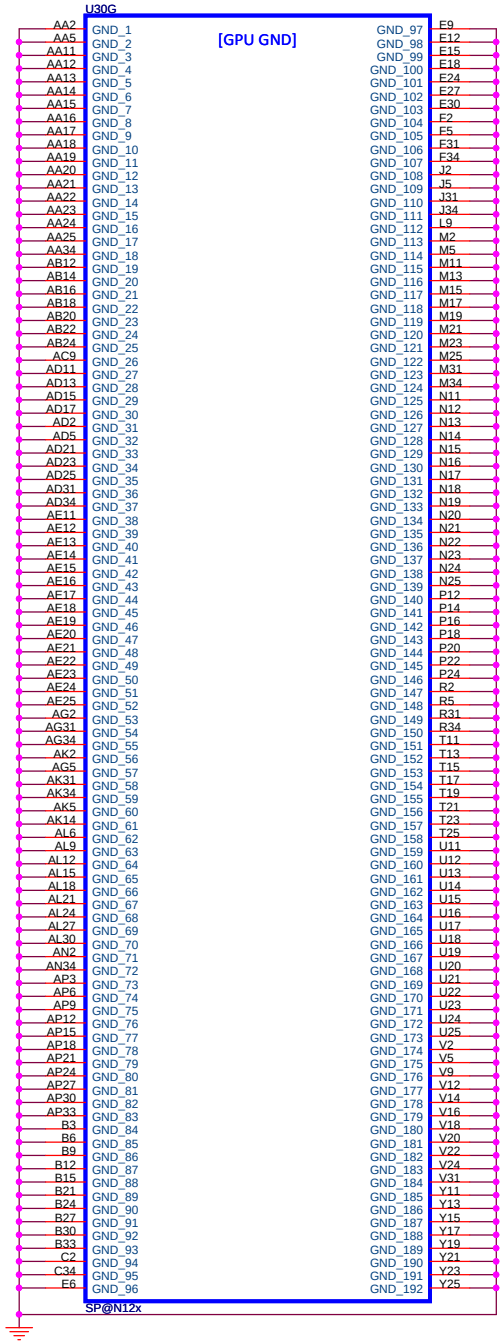
Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

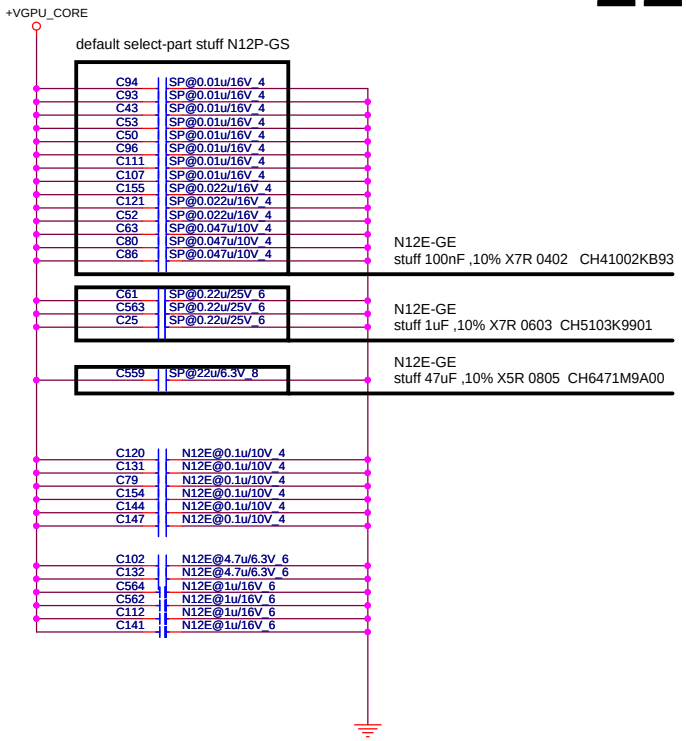
Date: Tuesday, February 22, 2011 Sheet 21 of 50











SPEC	GB2-128 12P-GS	GB3-128 12E-GE
10nF ,10% X7R 0402	8	
22nF ,10% X7R 0402	3	
47nF ,10% X7R 0402	3	
100nF ,10% X7R 0402	2	22
220nF ,10% X7R 0603	3	
1uF ,10% X7R 0603	1	8
4.7uF ,10% X5R 0603	1	3
10uF ,10% X5R 0805	2	2
22uF ,10% X5R 0805	1	
47uF ,10% X5R 0805	1	2
470uF	1	

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PROJECT : ZYG

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A

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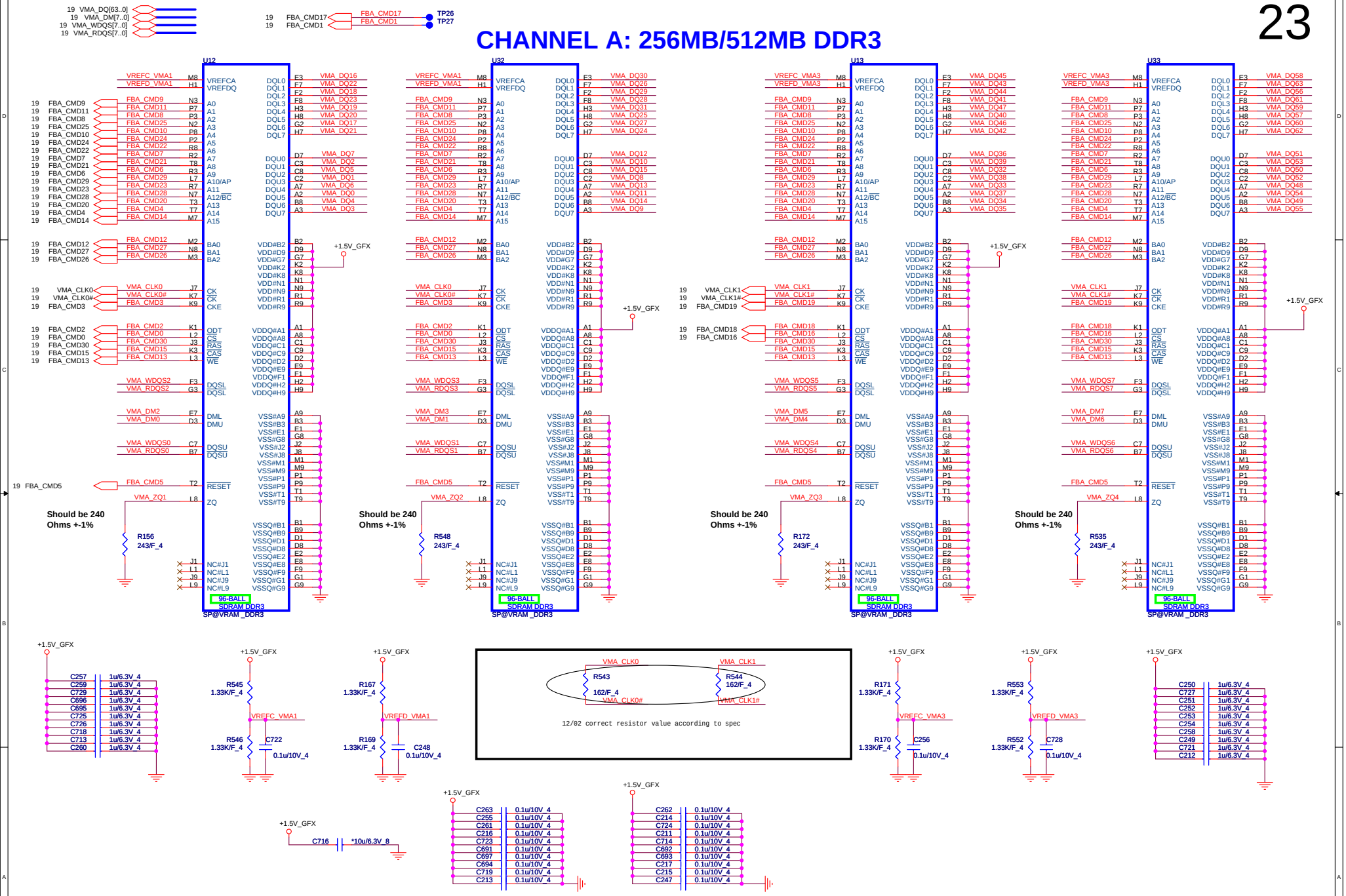
CHANNEL A: 256MB/512MB DDR3



A-stage	SKU1	SKU2	SKU3	SKU4
GPU	N12E-GE	N12P-GS	N12P-GS	N12P-GS (dGPU)
VRAM	Hyinx 2G	Hynix 1G	Sam 2G	Hynix 2G

VRAM		Description	Vendor P/N	QCI	QCI B/S
Hynix	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)H5TQ1G63DFR-11C(FBGA)STNBSQ	H5TQ1G63DFR-11C	AKD5LZWTW02	AKD5LZWTW05
Samsung	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)K4W1G1646G-BC11 STN BSQ	K4W1G1646G-BC11	AKD5EGGT500	AKD5EGGT503
Hynix	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)H5TQ2G63BFR-11C(FBGA)STNBSQ	H5TQ2G63BFR-11C	AKD5MGWTW00	AKD5MGWTW03
Samsung	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)K4W2G1646C-HC11(FBGA)STNBSQ	K4W2G1646C-HC11	AKD5MGWT500	AKD5MGWT503

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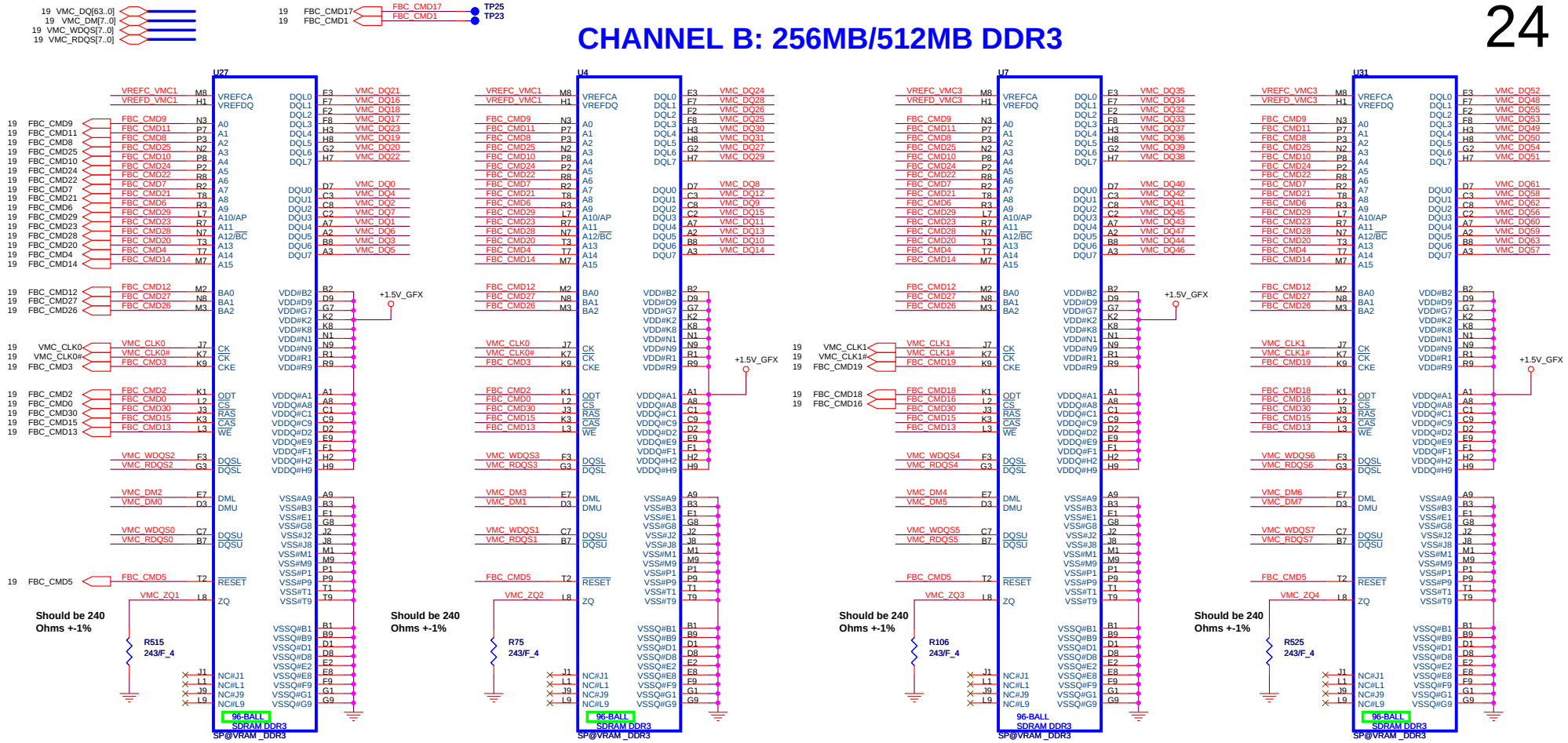
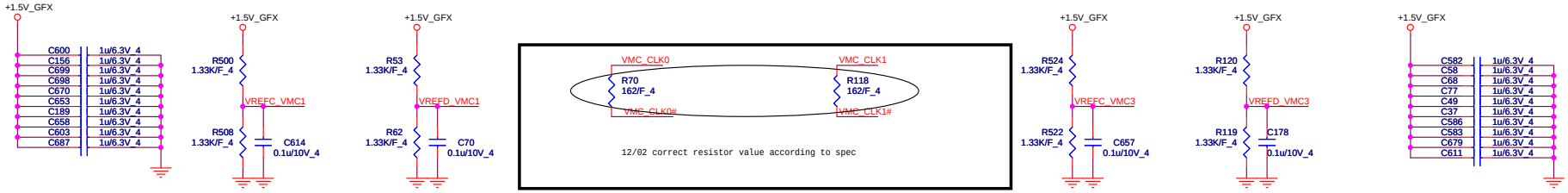
PROJECT : ZY6

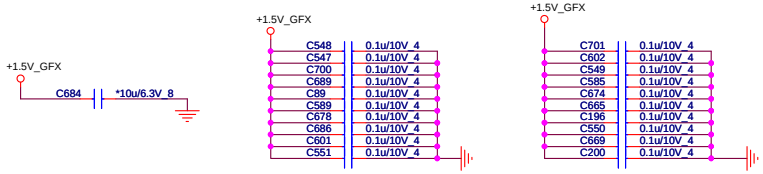
Size | Document Number: DGPU Memory 1/2 (DDR3) | Rev 1A

Date: Tuesday, February 22, 2011 | Sheet 23 of 50

CHANNEL B: 256MB/512MB DDR3







A-stage	SKU1	SKU2	SKU3	SKU4
GPU	N12E-GE	N12P-GS	N12P-GS	N12P-GS (dGPU)
VRAM	Hyinx 2G	Hynix 1G	Sam 2G	Hynix 2G

VRAM		Description	Vendor P/N	QCI	QCI B/S
Hynix	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)H5TQ1G63DFR-11C(FBGA)STNBSQ	H5TQ1G63DFR-11C	AKD5LZWTW02	AKD5LZWTW05
Samsung	DDR3 64Mx16x8, 1GB,900MHz	IC SDRAM(96P)K4W1G1646G-BC11 STN BSQ	K4W1G1646G-BC11	AKD5EGGT500	AKD5EGGT503
Hynix	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)H5TQ2G63BFR-11C(FBGA)STNBSQ	H5TQ2G63BFR-11C	AKD5MGWTW00	AKD5MGWTW03
Samsung	DDR3 128Mx16x8, 2GB,900MHz	IC SDRAM(96P)K4W2G1646C-HC11(FBGA)STNBSQ	K4W2G1646C-HC11	AKD5MGWT500	AKD5MGWT503

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PROJECT : ZY6

Size | Document Number: DGPU Memory 2/2 (DDR3) | Rev 1A

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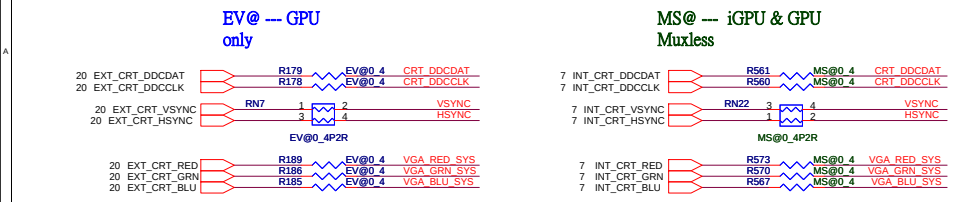
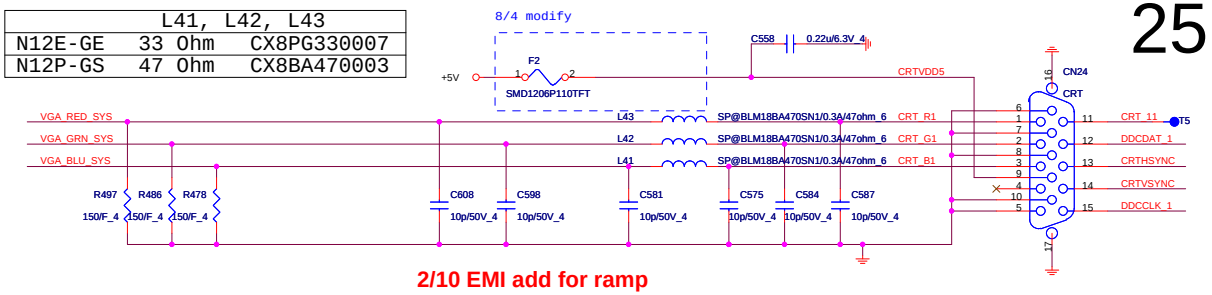
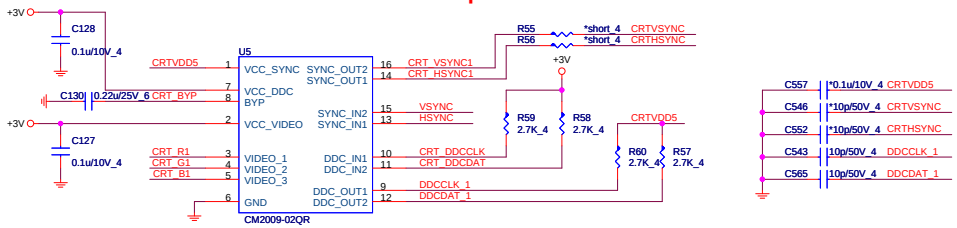
CRT

L41, L42, L43		
N12E-GE	33 Ohm	CX8PG330007
N12P-GS	47 Ohm	CX8BA470003

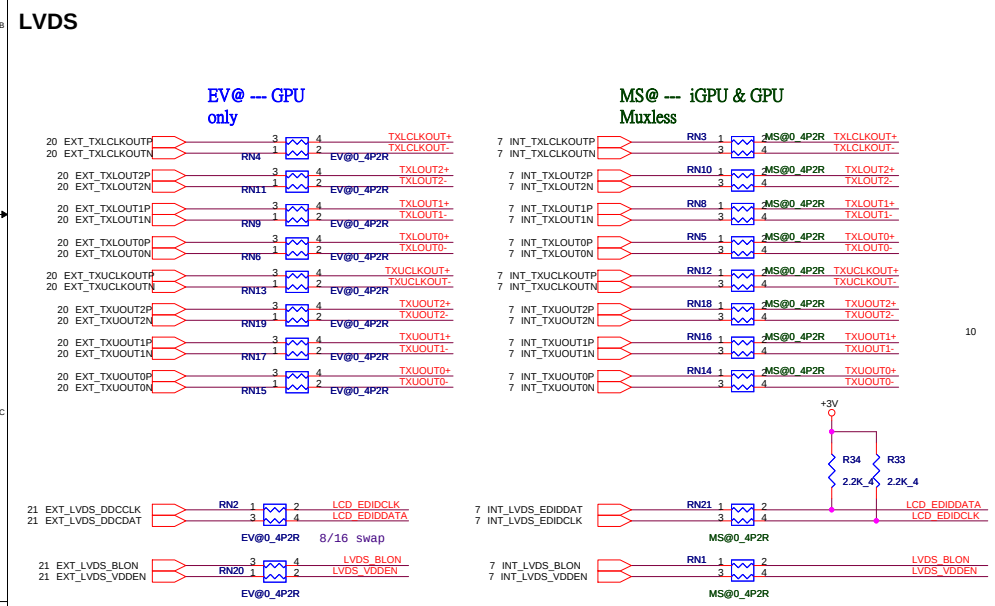


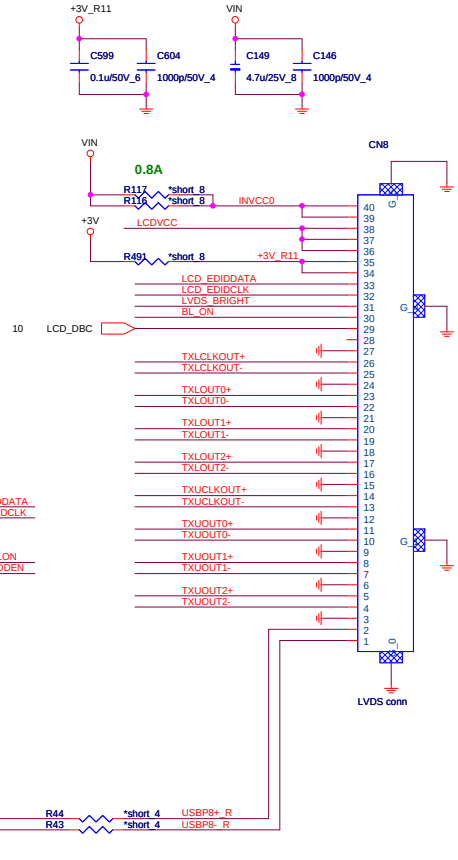


2/10 EMI add for ramp

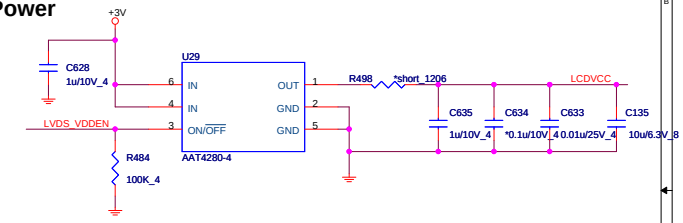


LVDS

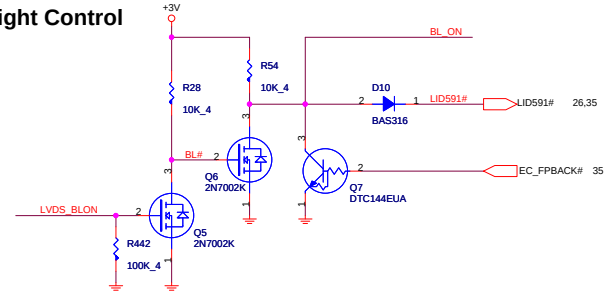


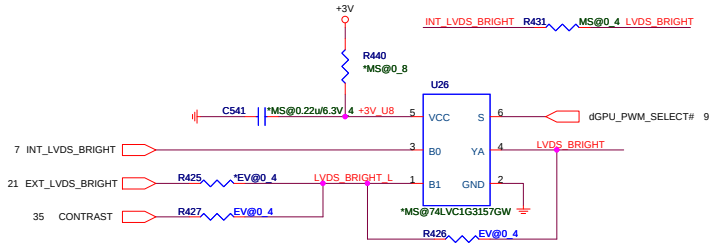


LCD Power



Backlight Control





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PROJECT : ZYG

Size	Document Number	Rev
	CRT/LVDS/LID	1A

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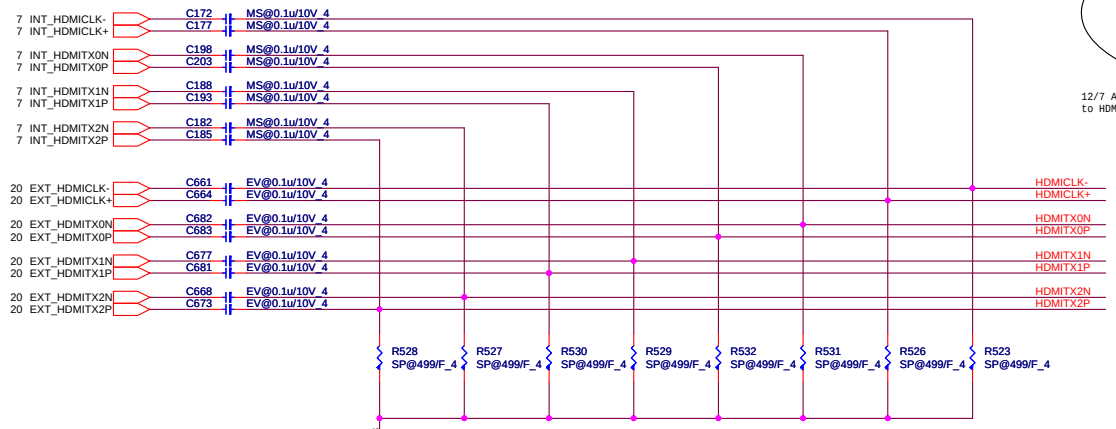
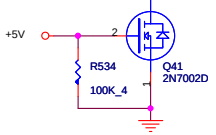
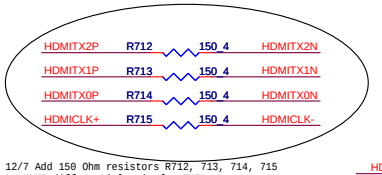
EV@ --- GPU
MS@ --- iGPU & GPU
Muxless



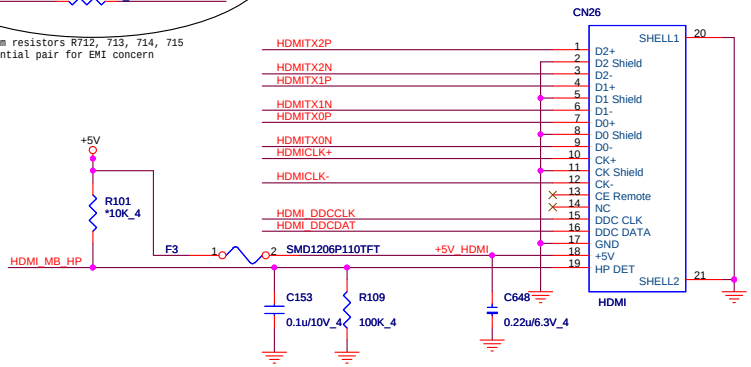


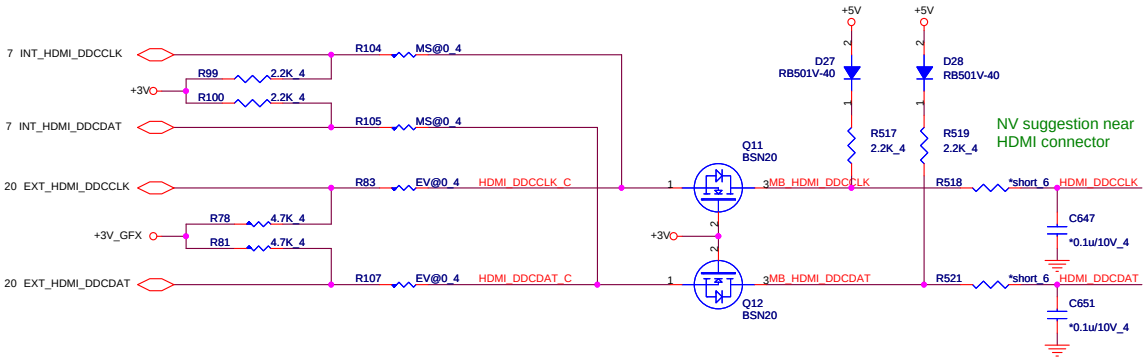
SP@ ---
MS(CS16802JB27--680ohm)
EV(CS14992FB24--499ohm)



12/7 Add 150 Ohm resistors R712, 713, 714, 715 to HDMI differential pair for EMI concern

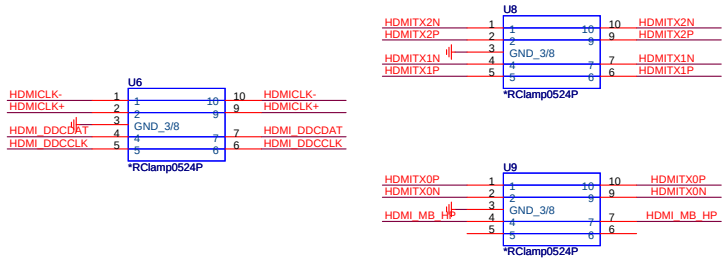
HDMI connector





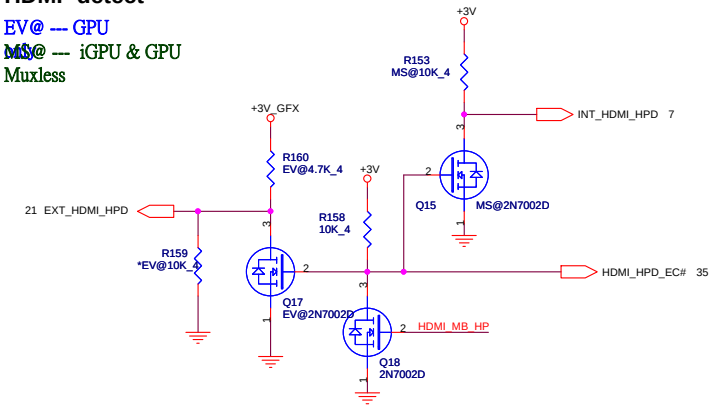
NV suggestion near HDMI connector

ESD Protect

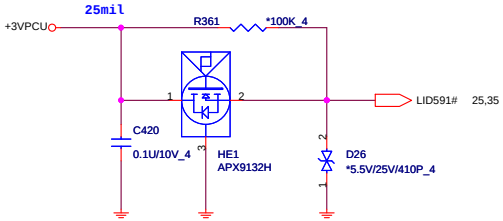


HDMI -detect

EV@ --- GPU
MS@ --- iGPU & GPU
Muxless



Lid Switch (Hall sensor)

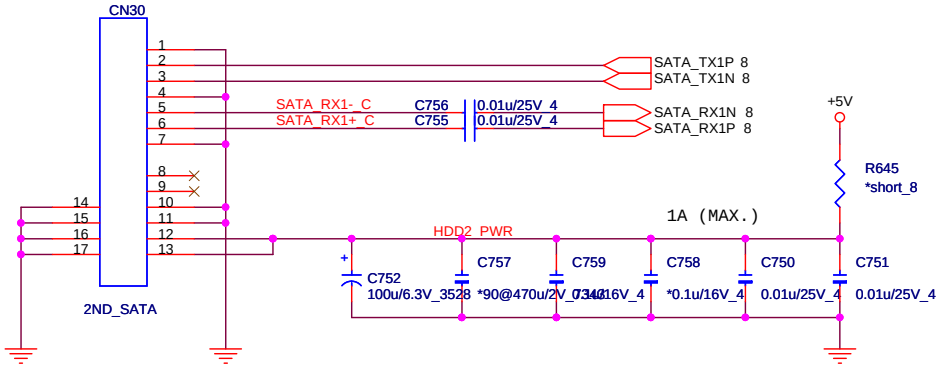


Quanta Computer Inc.
PROJECT : ZYG

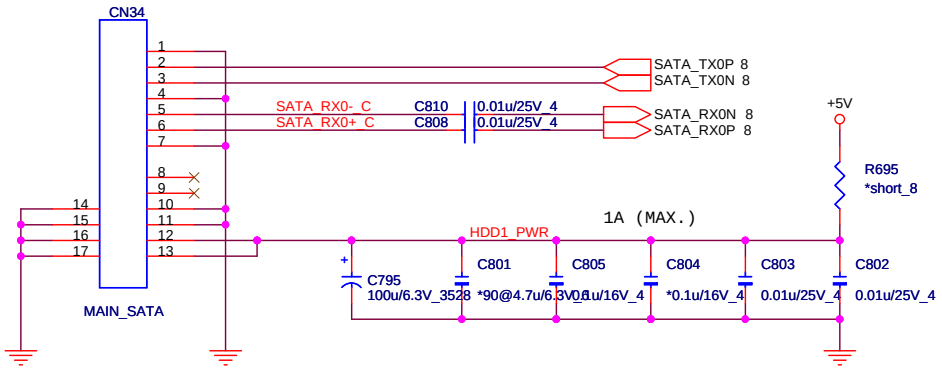
Size	Document Number	Rev
	HDMI/ Hall Sensor	1A

Date: Wednesday, February 23, 2011 Sheet 26 of 50

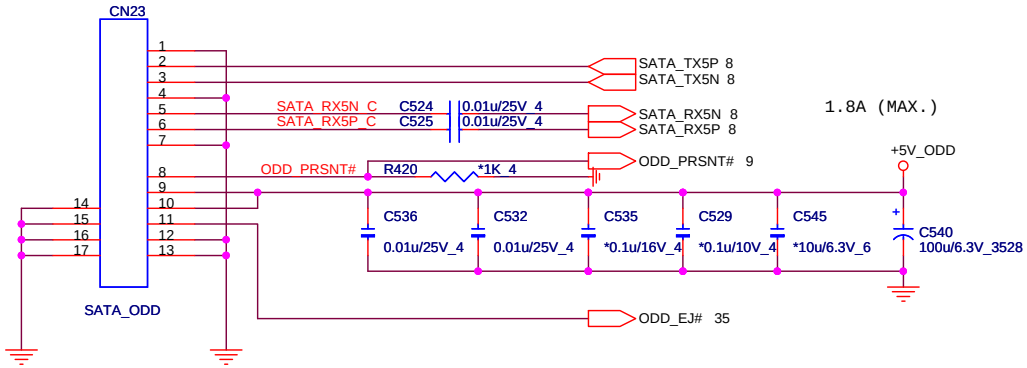
2nd SATA HDD (edge of board)



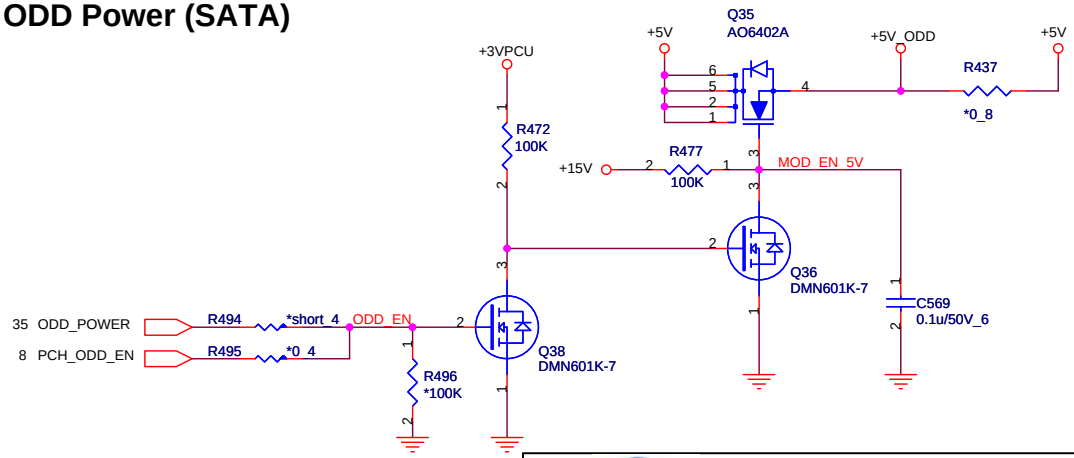
MAIN SATA HDD



ODD (SATA)



ODD Power (SATA)



Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	SATA-HDD/ODD	1A

Date: Tuesday, February 22, 2011 Sheet 27 of 50

MINI Wireless And Debug

12/8 Unmount R386, 393, mount R 385, 387, 391 for Intel WiDi WLAN card

+3.3V: 2700mA
+1.5V:500mA

3,9,18,31,32,33,35 PLTRST#
9 CLK_LPC_DEBUG
R386 *0_4 CL_DATA1_WLAN
R393 *0_4 CL_CLK1_WLAN

34,35 BT_POWERON#
9 CL_RST1#
9 CL_DAT1
9 CL_CLK1
R384 *0_4 BT_POWERON# R
R385 0_4 CL_RST1# WLAN
R387 0_4 CL_DATA1_WLAN
R391 0_4 CL_CLK1_WLAN

+3V_MINI1

9 PCIE_TX6P
9 PCIE_TX6N
9 PCIE_RX6P
9 PCIE_RX6N
9 CLK_PCIE_WLANP
9 CLK_PCIE_WLANN
9 PCIE_CLKREQ_WLAN#
PCIE_CLKREQ_WLAN#
PCIE_WAKE# R

CN22
MiniCard_WLAN

Pin	Signal	Pin	Signal
51	Reserved	52	+3.3V
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	LED_WPAN#
43	Reserved	44	LED_WLAN#
41	NC	42	LED_WWAN#
39	NC	40	GND
37	Reserved	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	NC	20	W_DISABLE#
17	NC	18	GND
15	GND	16	NC
13	REFCLK+	14	NC
11	REFCLK-	12	NC
9	GND	10	NC
7	CLKREQ#	8	NC
5	Reserved	6	+1.5V
3	Reserved	4	GND
1	WAKE#	2	+3.3V
54	FIX	53	FIX

+1.5V
+3V
R392 *0_8
R383 *short_8
+1.5V_MINI1
+3V_MINI1

RF_LED# 34
USBP10+ 9
USBP10- 9
CLK_SDATA
CLK_SCLK
CLK_SDATA 9,13,14,15,16
CLK_SCLK 9,13,14,15,16
PLTRST#
PLTRST# 3,9,18,31,32,33,35
RF_EN 35

A_LFRAME# R R409 *short_4 LPC_LFRAME# 8,35
A_LAD3 R R410 *short_4 LPC_LAD3 8,35
A_LAD2 R R412 *short_4 LPC_LAD2 8,35
A_LAD1 R R414 *short_4 LPC_LAD1 8,35
A_LAD0 R R419 *short_4 LPC_LAD0 8,35

+3V_MINI1
Q32 *DTC144EUA
7,32,33 PCIE_WAKE#
PCIE_WAKE# R

+3V_MINI1
C463 *10u/6.3V_6
C464 4.7u/10V_6
C465 0.1u/16V_4

+3V_MINI1
C530 0.1u/16V_4
C517 0.1u/16V_4

+1.5V_MINI1
C466 *0.1u/10V_4
C510 *0.1u/10V_4
C473 *10u/6.3V_6

MINI GPS Module

GPS@BKP1608HS181T/1.5A/180ohm_6
+3V_MINI2
L38
+3V_GPS
C544 *GPS@10u/6.3V_6
C542 GPS@0.1u/16V_4

9 PCIE_TX3P
9 PCIE_TX3N
9 PCIE_RX3P
9 PCIE_RX3N
9 CLK_PCIE_GPSP
9 CLK_PCIE_GPSN
9 PCIE_CLKREQ_GPS#

CN25
GPS@MiniCard_GPS

Pin	Signal	Pin	Signal
51	Reserved	52	+3.3V
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	LED_WPAN#
43	Reserved	44	LED_WLAN#
41	NC	42	LED_WWAN#
39	NC	40	GND
37	Reserved	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	NC	20	W_DISABLE#
17	NC	18	GND
15	GND	16	NC
13	REFCLK+	14	NC
11	REFCLK-	12	NC
9	GND	10	NC
7	CLKREQ#	8	NC
5	Reserved	6	+1.5V
3	Reserved	4	GND
1	WAKE#	2	+3.3V
54	FIX	53	FIX

+1.5V
+3V
R473 *GPS@0_8
R443 *GPS@short_8
+1.5V_MINI2
+3V_MINI2

USBP13+ 9
USBP13- 9
CLK_SDATA
CLK_SCLK
PLTRST#

+3V_MINI2
C553 *GPS@10u/6.3V_6
C556 *GPS@4.7u/10V_6
C18 GPS@0.1u/16V_4

+3V_MINI2
C643 GPS@0.1u/16V_4
C612 GPS@0.1u/16V_4

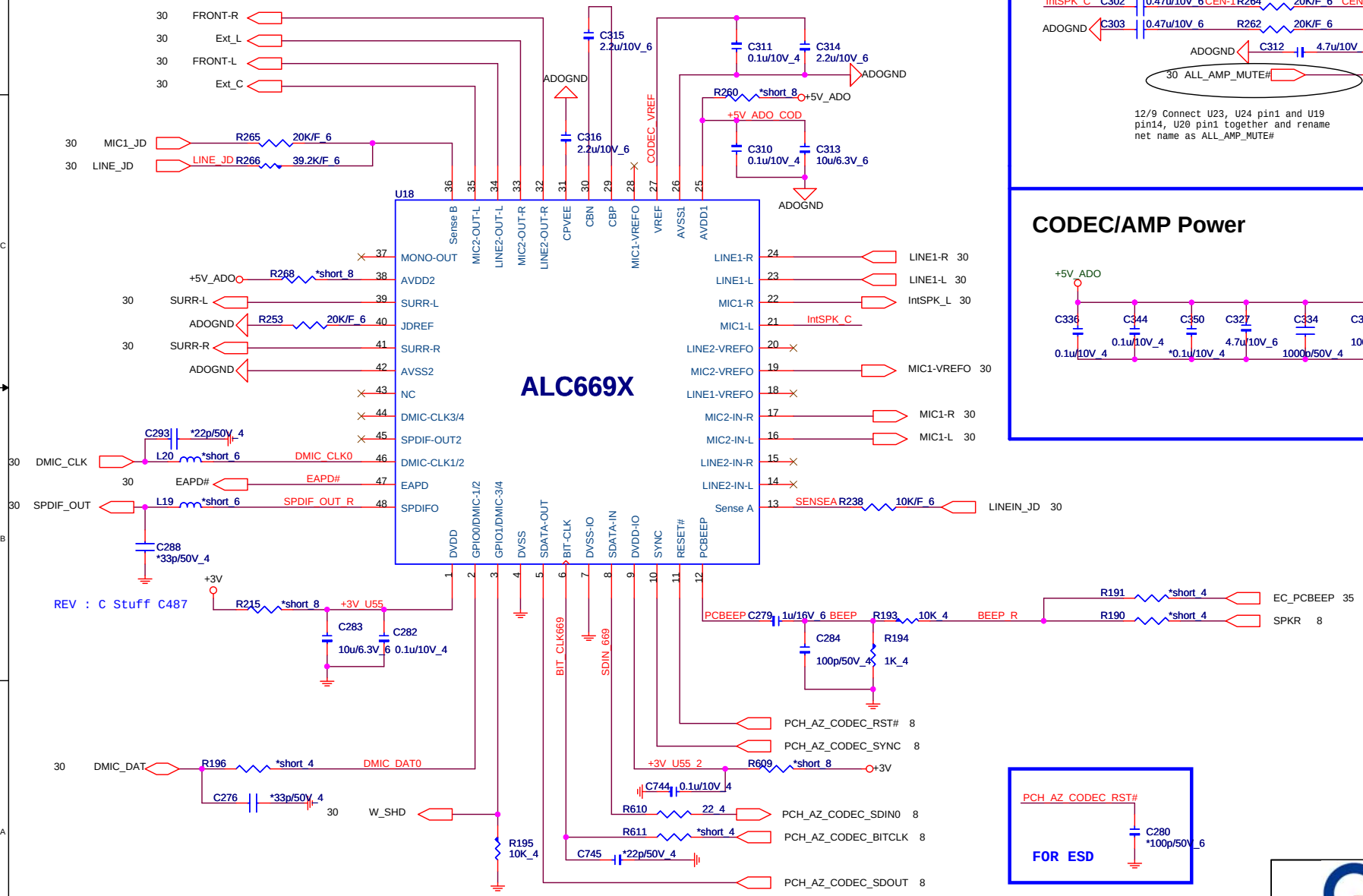
+1.5V_MINI2
C642 *GPS@0.1u/10V_4
C609 *GPS@0.1u/10V_4
C566 *GPS@10u/6.3V_6

Quanta Computer Inc.
PROJECT : ZYG

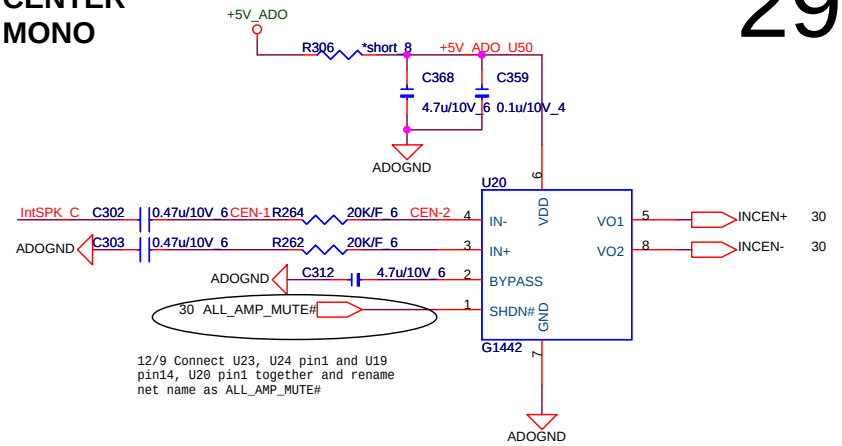
Size	Document Number	Rev
	MINI PCI-E card/TV	1A

Date: Tuesday, February 22, 2011 Sheet 28 of 50

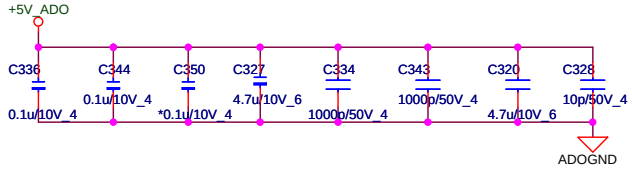
CODEC(ALC669X)



CENTER MONO



CODEC/AMP Power



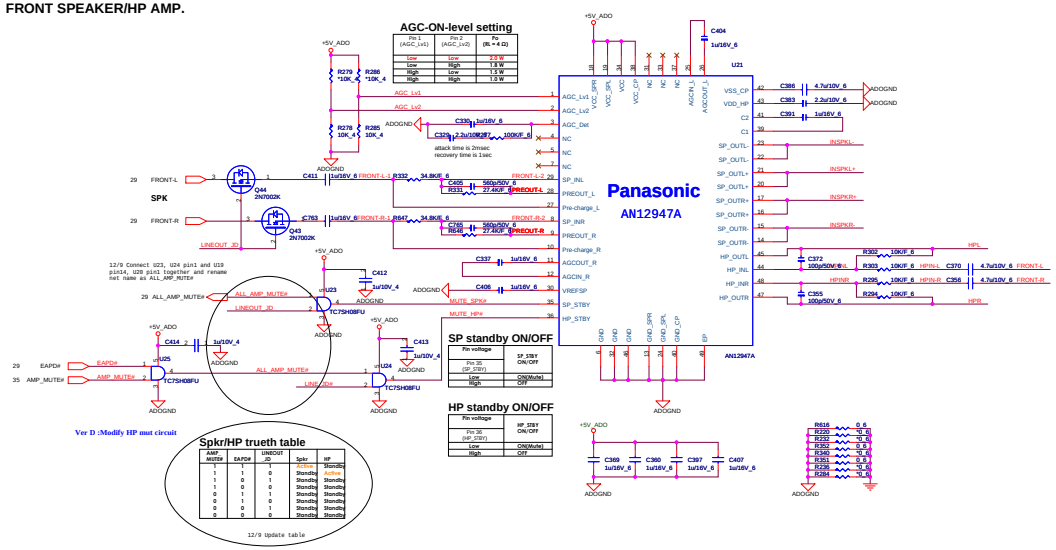
FOR ESD

PCH_AZ_CODEC_RST#

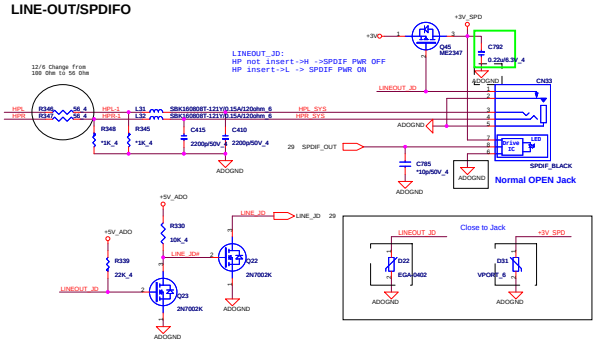
C280 *100p/50V_6

Quanta Computer Inc.		
PROJECT : ZYG		
Size	Document Number: REALTEK ALC889X/MONO-AMP	Rev 1A
Date: Tuesday, February 22, 2011	Sheet 29 of 50	

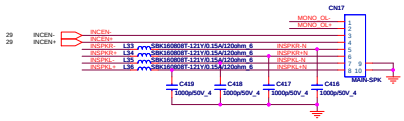
FRONT SPEAKER/HP AMP.



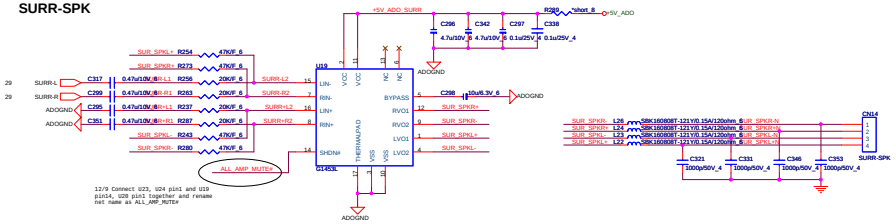
LINE-OUT/SPDIFO



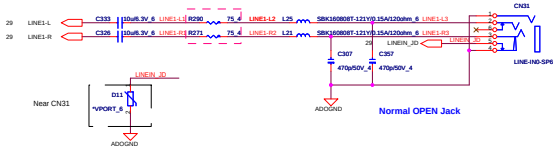
Main SPK/Center/Subwoofer



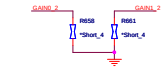
SURR-SPK



LINE IN



AMO GAIN



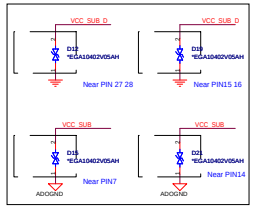
	GAIN1	GAIN0	Gain<dB>
default	0	0	29
	0	1	26
	1	0	32
	1	1	36

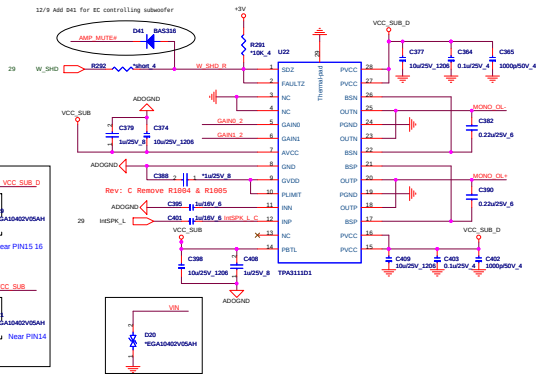
SUBWOOFER

LPF for fc(-3dB)=500Hz

SDZ ::shutdown signal for IC<LOW=disable , HIGH=enable>

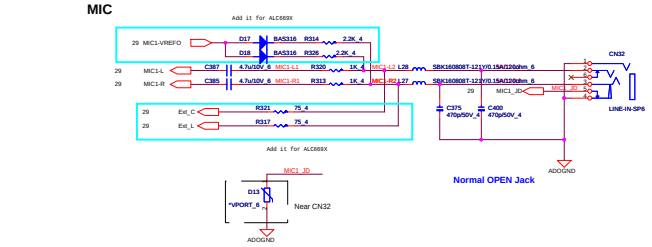
SHUTDOWN	TPA3110D1
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE



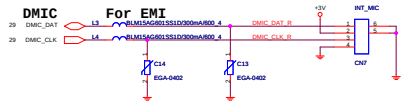


SUBWOOFER Power(AMP)

MIC



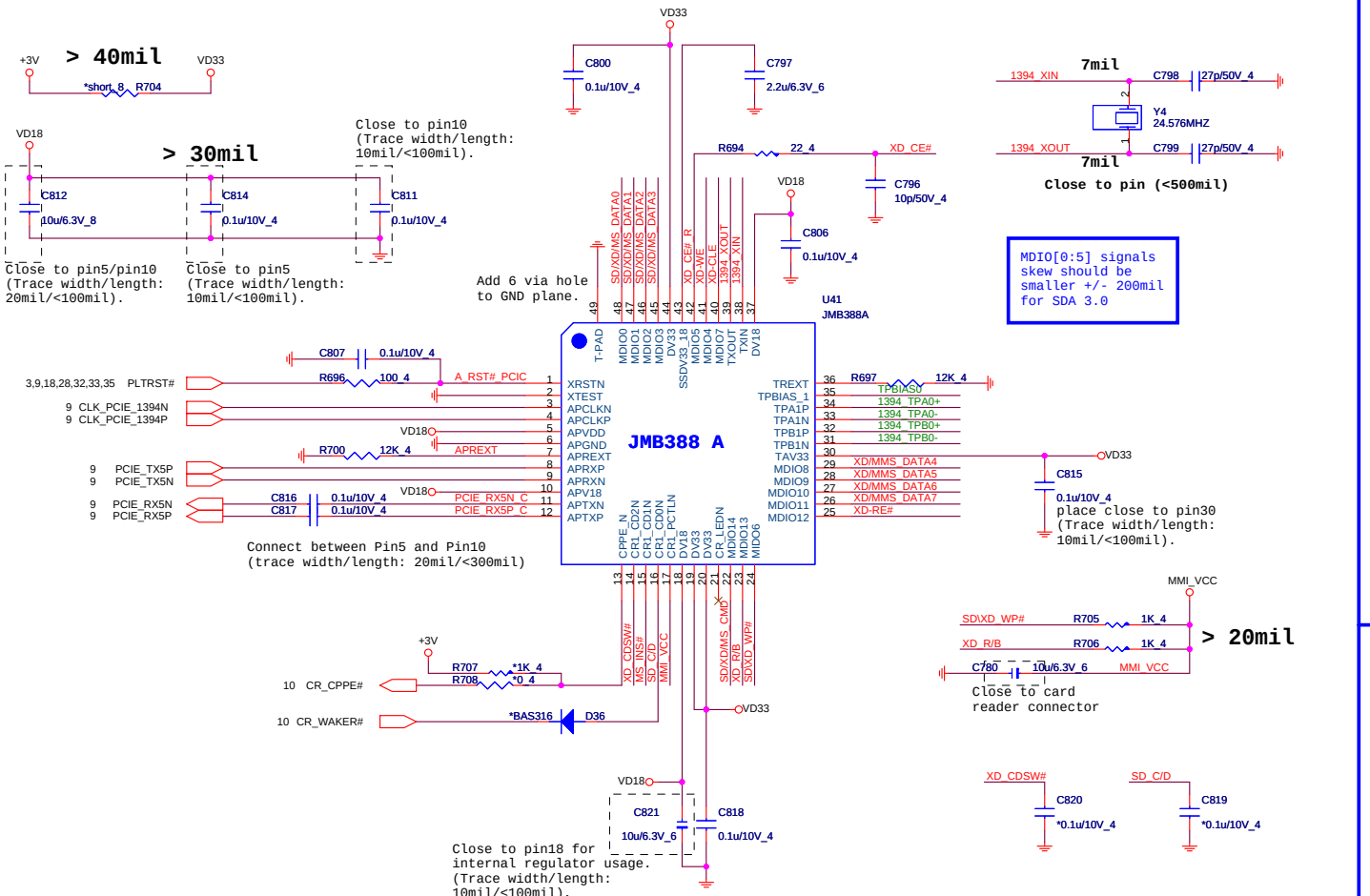
DMIC For EMI

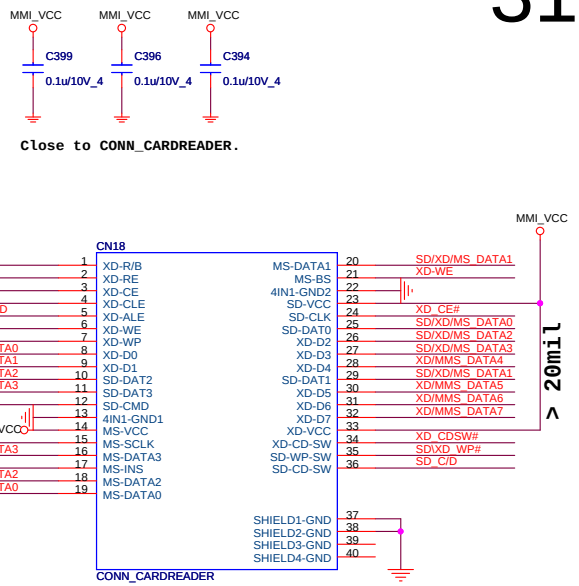


Quanta Computer Inc.		
PROJECT : ZY6		
Size	Document Number	Rev
	AMP/AUDIO JACK/WOOFER	1A
Date: Tuesday, February 22, 2011	Sheet 30 of 50	

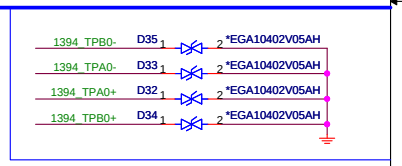
Card Reader (JMB388A)

Chip Note:
1. All component must be closed to chip.
2. APREXT(pin7) & TREXT(pin36) trace width/length: 10mil/< 250mil

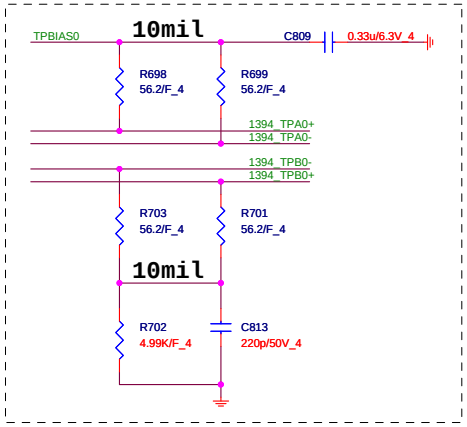




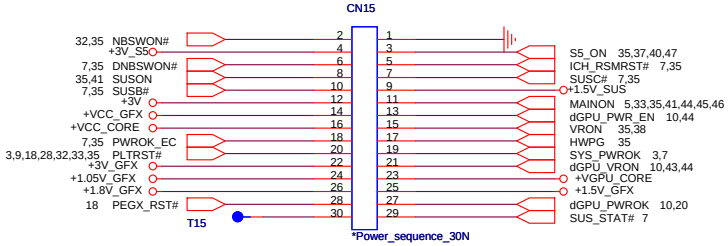
1394 [FIW]



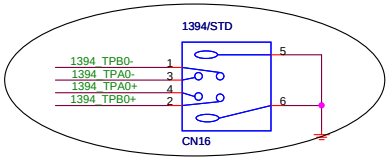
Close to Chip JMB388A



Power sequence



1/6 change 1394 connector fp and pin assignment



These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	Card Reader & 1394	1A

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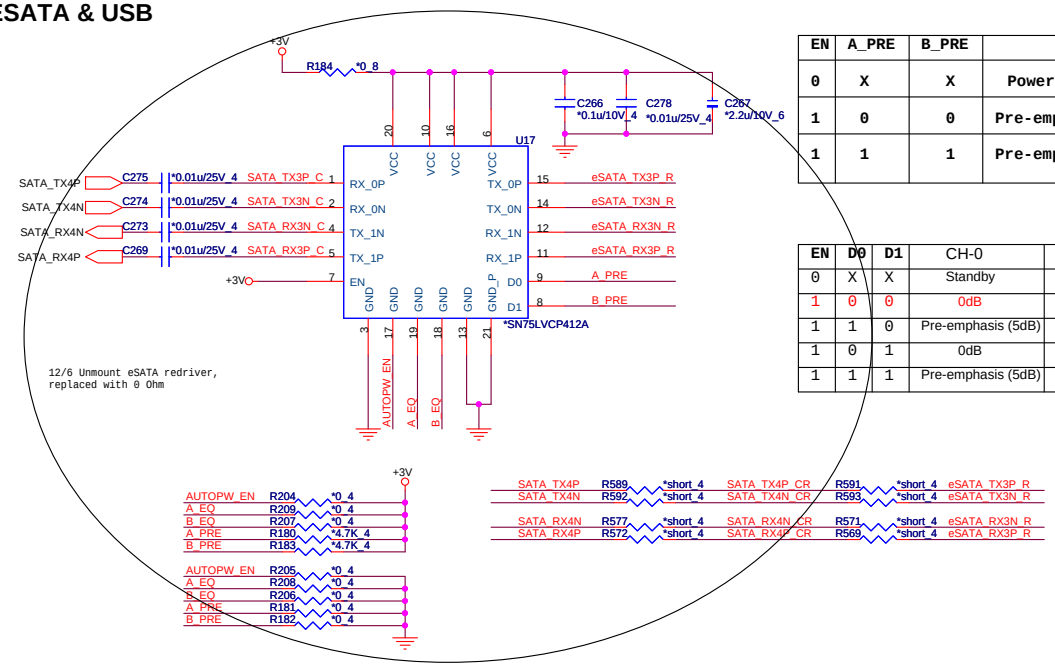
ESATA & USB

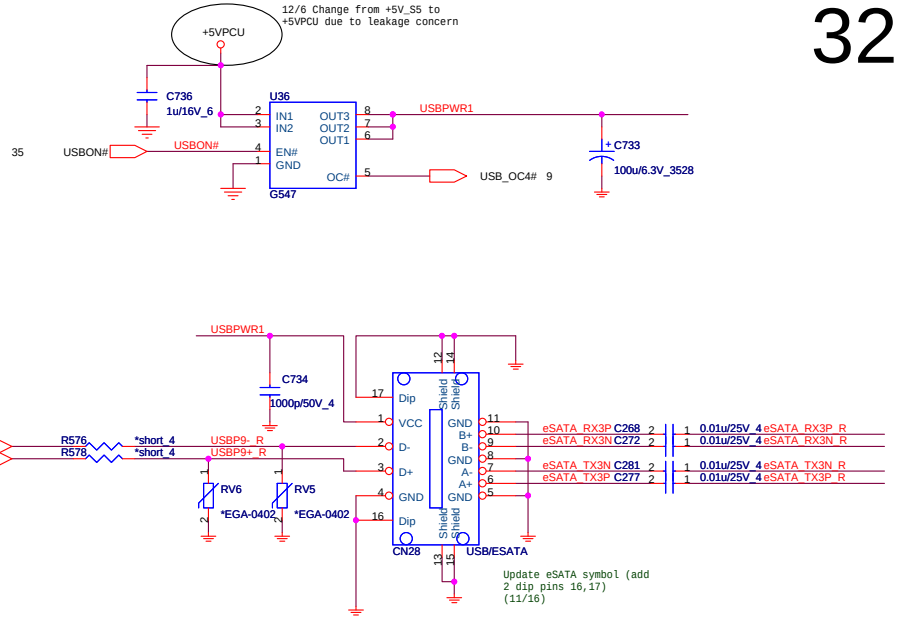


AL008511001

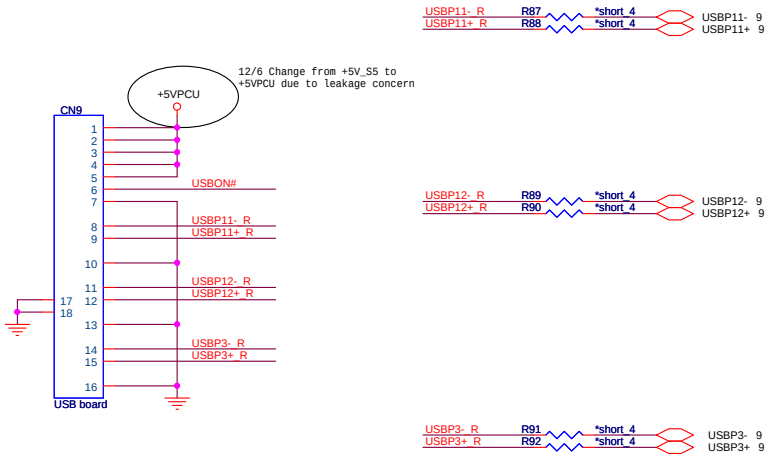
EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

ALLVC412000

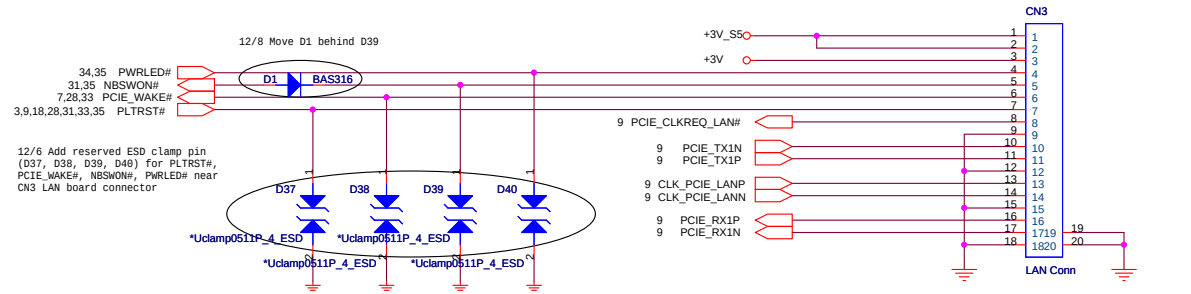
EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)



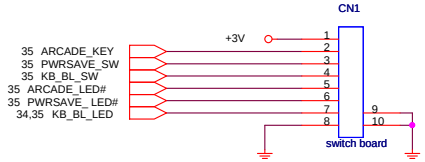
To USB DB



To PWR/LAN DB



To SW DB



Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	USB/eSATA/DB Conn.	1A

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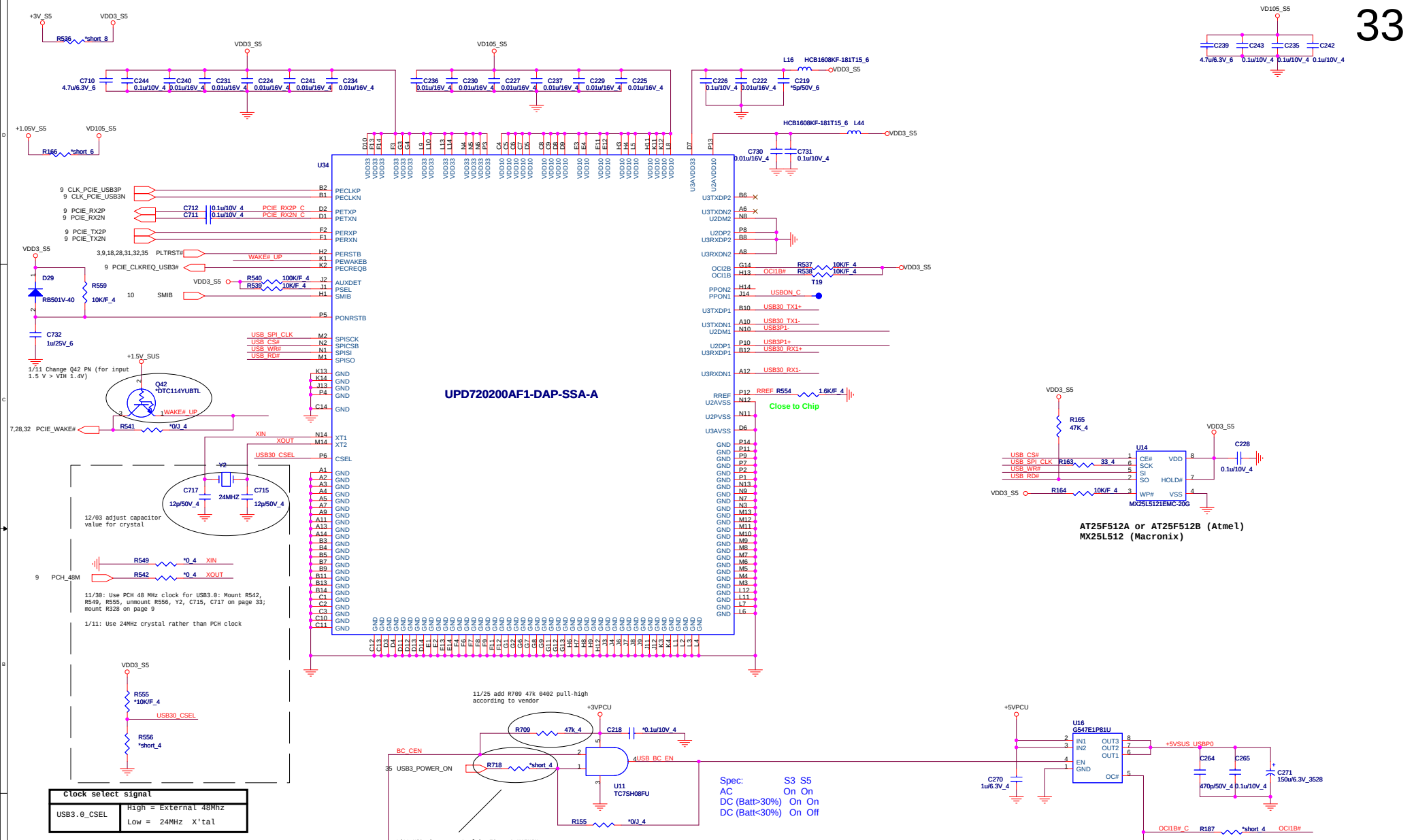


Clock select signal	
USB3.0_CSEL	High = External 48Mhz
	Low = 24MHz X'tal

	S3	S5
Spec:		
AC	On	On
DC (Batt>30%)	On	On
DC (Batt<30%)	On	Off

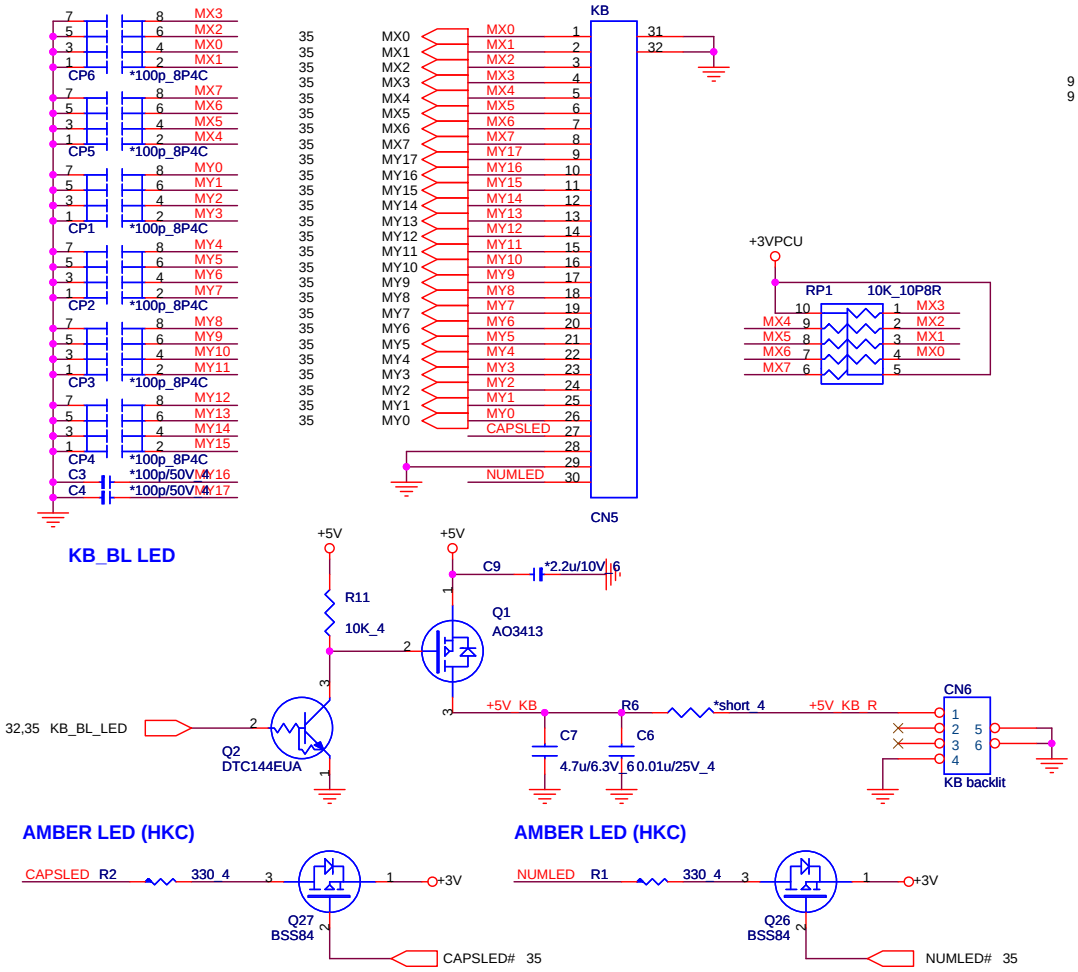
Quanta Computer Inc.

PROJECT : ZYG

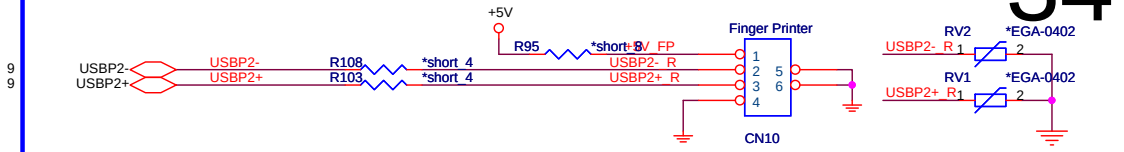
Size	Document Number	Rev
	USB 3.0	1A

Date: Tuesday, February 22, 2011 Sheet 33 of 50

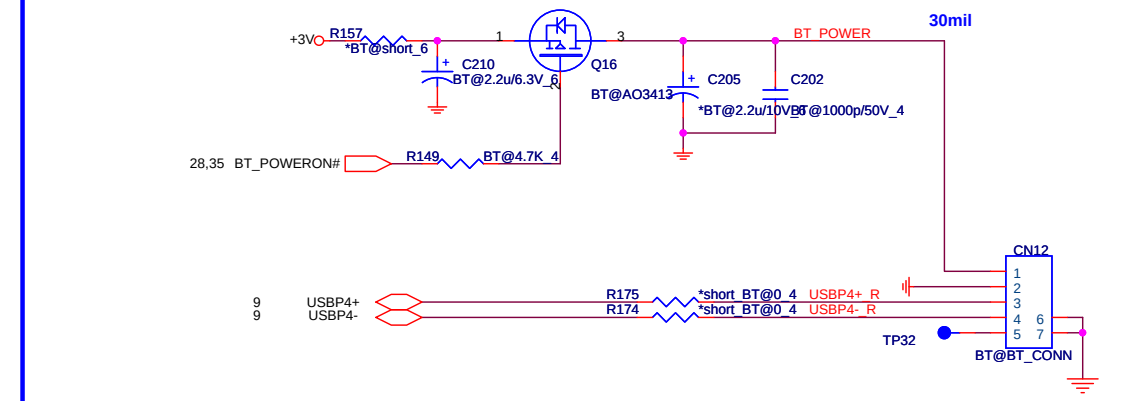
INT K/B



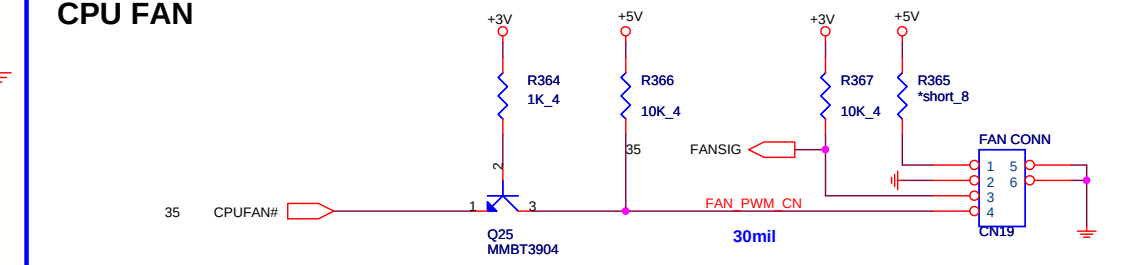
Finger-Printer



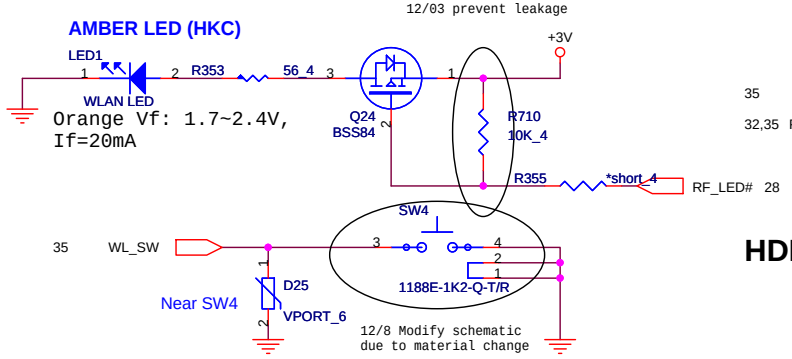
BLUETOOTH



CPU FAN

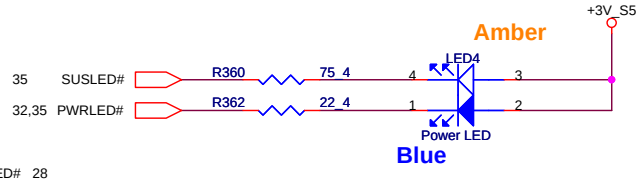


WL LED

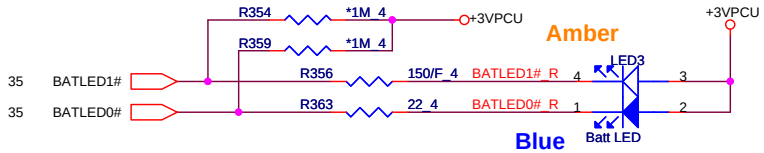


PWR LED

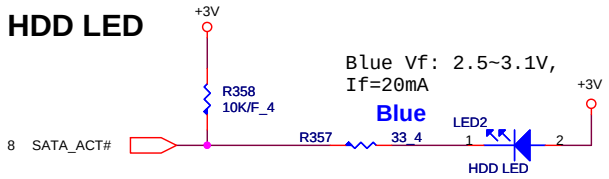
PWR: Blue Vf: 2.55~3.15V, If=20mA
SUS: Orange Vf=1.6~2.0V, If=20mA



Battery LED



HDD LED



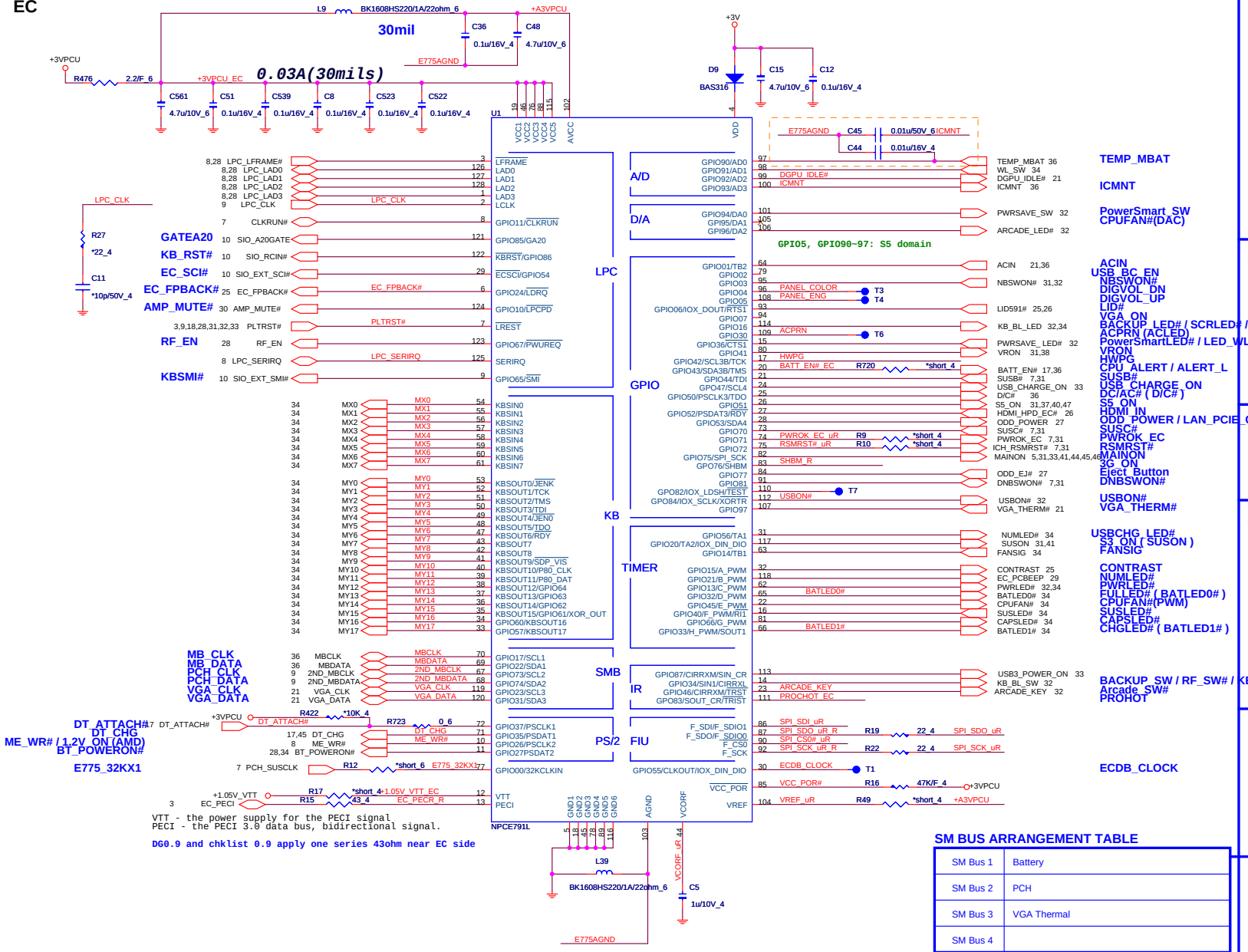
Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	KB/FAN/FP/BT/LED	1A

Date: Tuesday, February 22, 2011 Sheet 34 of 50

EC



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA Thermal
SM Bus 4	

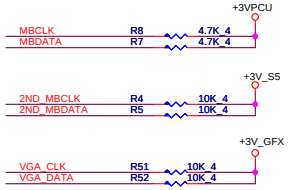
I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

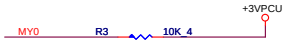
SHBM=0: Enable shared memory with host BIOS

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

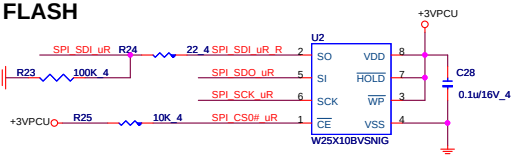
SM BUS PU



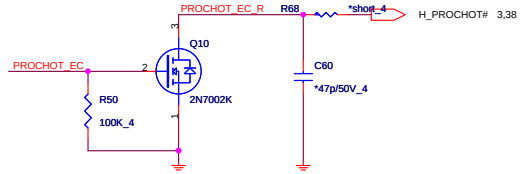
INTERNAL KEYBOARD STRIP SET



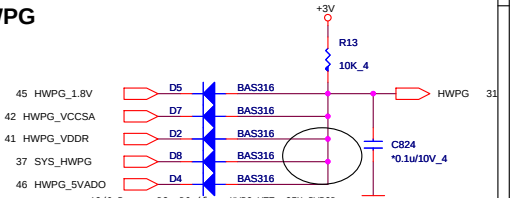
SPI FLASH



Winbond	W25X10BVSNIG	AKE35FN0N00
EON	EN25F10-100GIP	AKE35FN0Q00
AMIC	A25L010O-F	AKE35ZN0800



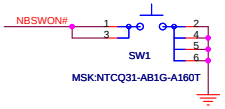
HWPG



12/6 Remove D3, D6 (from HWPG_VTT, GFX_PWRGD, because HWPG_VTT enables VCCSA, GFX_PWRGD connect to U42 on PCH page)

1/12 Add reserved 0.1uF C824 for ESD concern

POWER-ON Switch

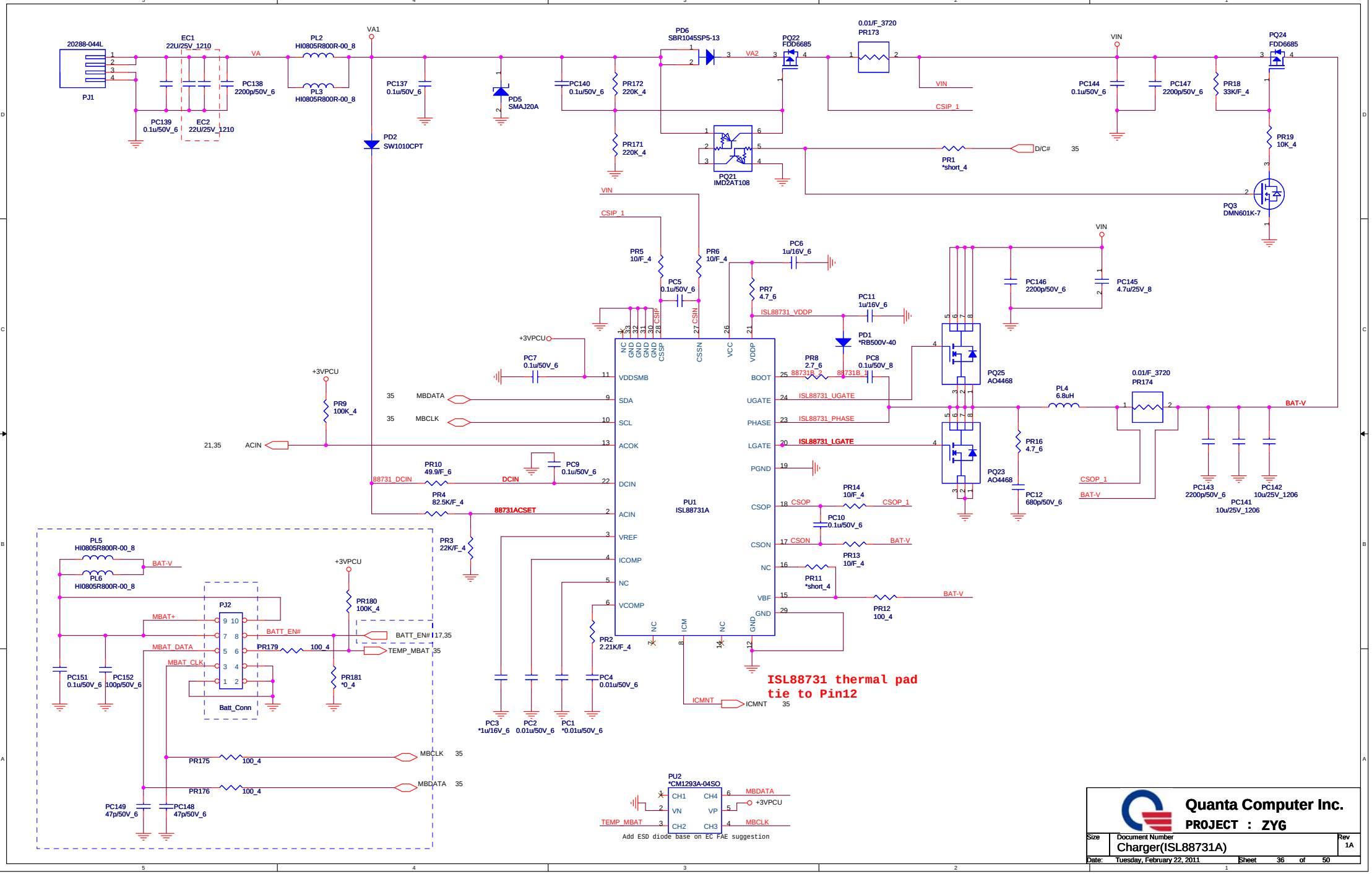


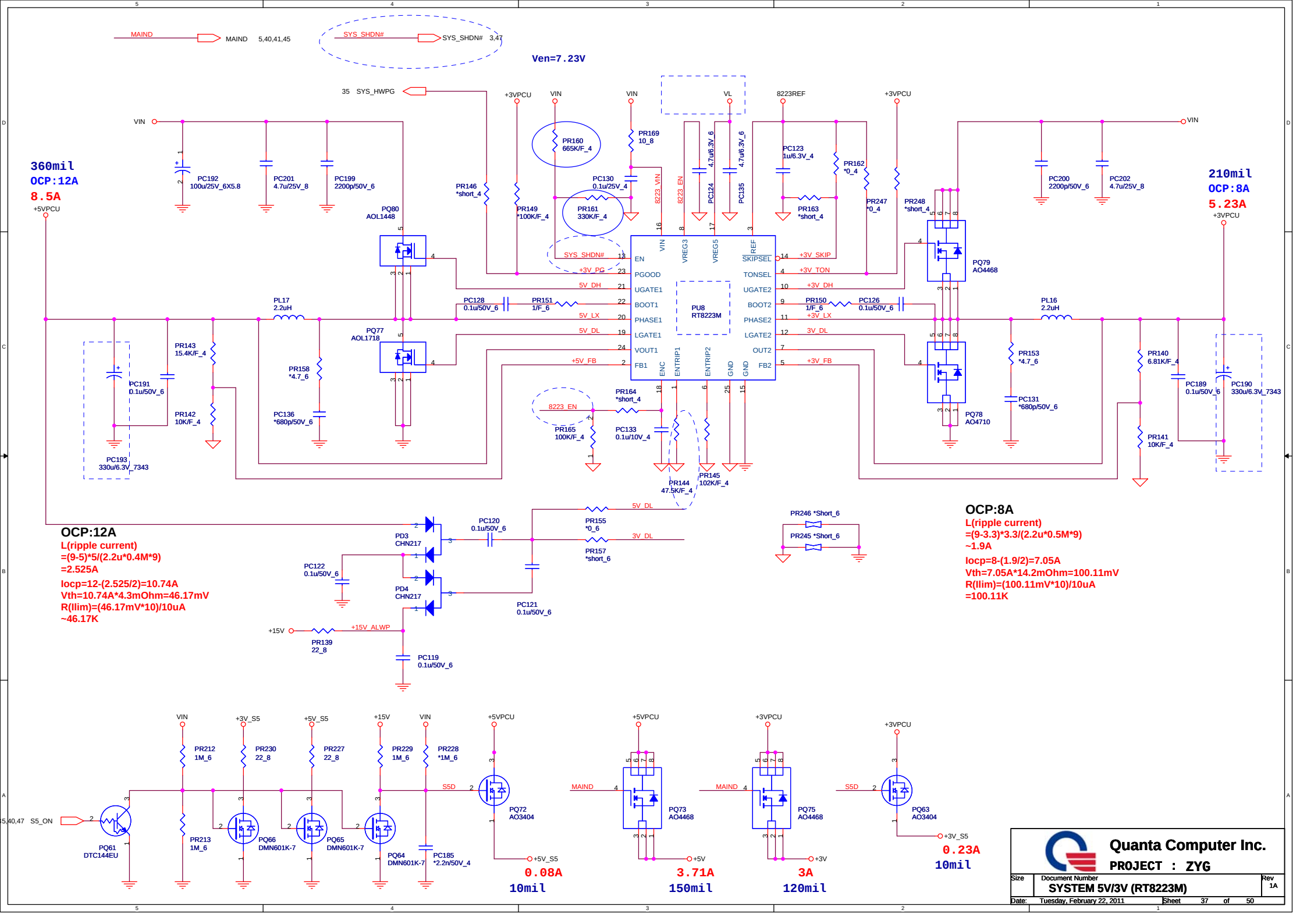
Quanta Computer Inc.

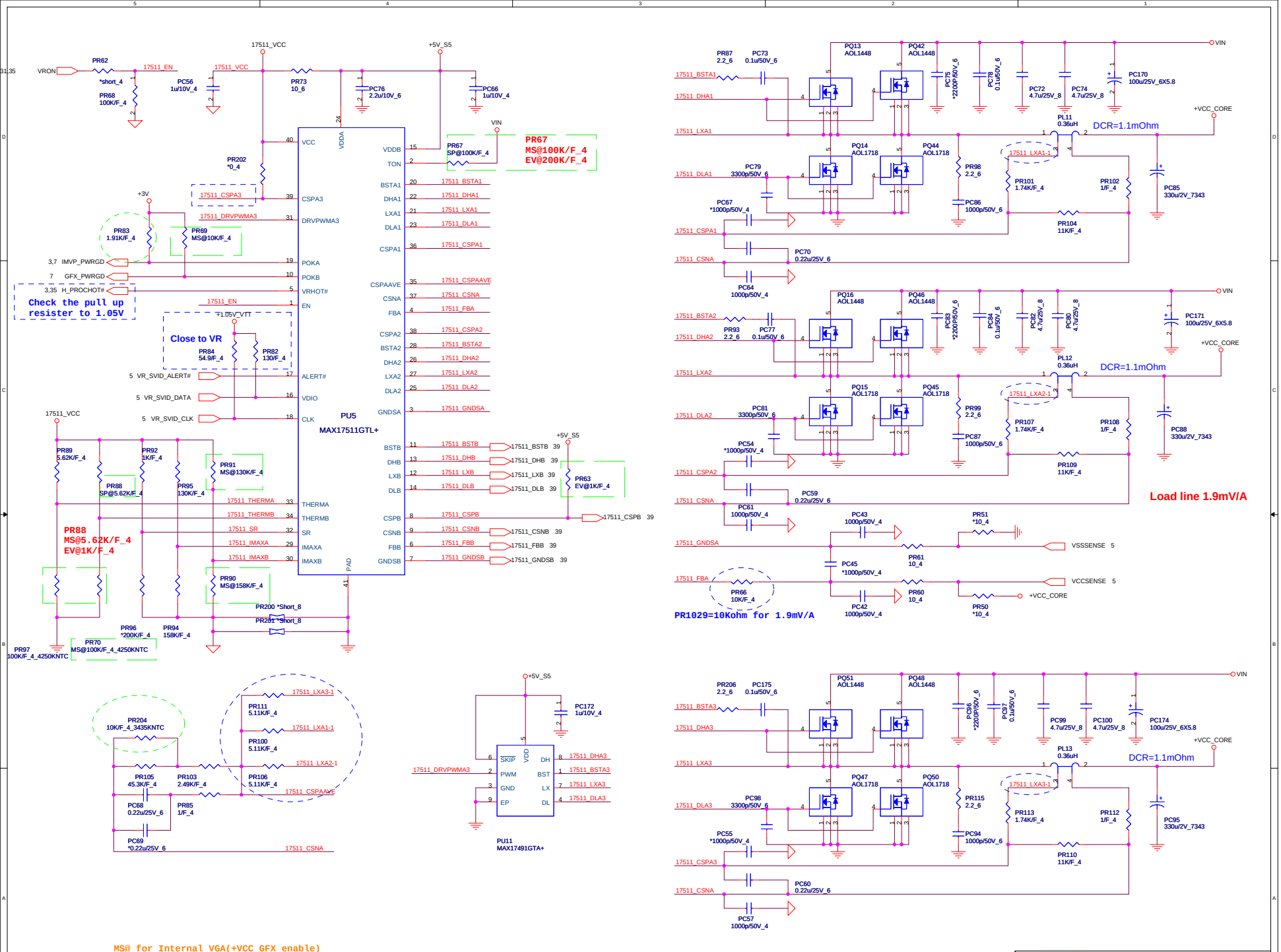
PROJECT : ZYG

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

Date: Tuesday, February 22, 2011 Sheet 35 of 50


20288-044L
PJ1
EC1
22U/25V_1210
EC2
22U/25V_1210
PC138
2200p/50V_6
PC139
0.1u/50V_6
PL2
HI0805R800R-00_8
PL3
HI0805R800R-00_8
VA
VA1
PC137
0.1u/50V_6
PD2
SW1010CPT
PD5
SMAJ20A
PC140
0.1u/50V_6
PR172
220K_4
PR171
220K_4
PD6
SBR1045SP5-13
VA2
PQ22
FDD6685
0.01/F_3720
PR173
VIN
CSIP_1
PQ21
IMD2AT108
PR1
*short_4
D/C#
35
PC144
0.1u/50V_6
PC147
2200p/50V_6
PR18
33K/F_4
PQ24
FDD6685
PR19
10K_4
PQ3
DMN601K-7
PR5
10/F_4
PR6
10/F_4
PC5
0.1u/50V_6
PC6
1u/16V_6
PR7
4.7_6
PC11
1u/16V_6
ISL88731_VDDP
PD1
*RB500V-40
PC8
0.1u/50V_8
PR8
2.7_6
88731B_2
88731B_1
PC146
2200p/50V_6
PC145
4.7u/25V_8
PQ25
AO4468
PQ23
AO4468
PL4
6.8uH
0.01/F_3720
PR174
BAT-V
PR16
4.7_6
PC12
680p/50V_6
CSOP_1
PC143
2200p/50V_6
PC141
10u/25V_1206
PC142
10u/25V_1206
+3VPCU
PC7
0.1u/50V_6
PR9
100K_4
35
MBDATA
35
MBCLK
21,35
ACIN
PR10
49.9/F_6
88731_DCIN
DCIN
PC9
0.1u/50V_6
PR4
82.5K/F_4
88731ACSET
PR3
22K/F_4
PU1
ISL88731A
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PR14
10/F_4
PC10
0.1u/50V_6
PR13
10/F_4
PR11
*short_4
PR12
100_4
PR2
2.21K/F_4
PC4
0.01u/50V_6
PC3
*1u/16V_6
PC2
0.01u/50V_6
PC1
*0.01u/50V_6
ICMNT
ICMNT
35
ISL88731 thermal pad
tie to Pin12
PL5
HI0805R800R-00_8
PL6
HI0805R800R-00_8
PJ2
Batt_Conn
MBAT+
MBAT_DATA
MBAT_CLK
BATT_EN#
PR179
100_4
BATT_EN#
17,35
TEMP_MBAT
35
PR180
100K_4
PR181
*0_4
PC151
0.1u/50V_6
PC152
100p/50V_6
PR175
100_4
MBCLK
35
PR176
100_4
MBDATA
35
PC149
47p/50V_6
PC148
47p/50V_6
PU2
*CM1293A-04SO
CH1
VN
CH2
CH4
VP
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZYG
Size
Document Number
Charger(ISL88731A)
Rev
1A
Date: Tuesday, February 22, 2011
Sheet 36 of 50


MAIND
MAIND 5,40,41,45
SYS_SHDN#
SYS_SHDN# 3,47
Ven=7.23V
35 SYS_HWPG
360mil
OCP:12A
8.5A
210mil
OCP:8A
5.23A
PU8
RT8223M
PQ80
AOL1448
PQ77
AOL1718
PQ79
AO4468
PQ78
AO4710
PD3
CHN217
PD4
CHN217
OCP:12A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=12-(2.525/2)=10.74A
Vth=10.74A*4.3mOhm=46.17mV
R(Ilim)=(46.17mV*10)/10uA
~46.17K
OCP:8A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=8-(1.9/2)=7.05A
Vth=7.05A*14.2mOhm=100.11mV
R(Ilim)=(100.11mV*10)/10uA
=100.11K
PQ61
DTC144EU
PQ66
DMN601K-7
PQ65
DMN601K-7
PQ64
DMN601K-7
PQ72
AO3404
PQ73
AO4468
PQ75
AO4468
PQ63
AO3404
0.08A
10mil
3.71A
150mil
3A
120mil
0.23A
10mil
Quanta Computer Inc.
PROJECT : ZYG
Size
Document Number
SYSTEM 5V/3V (RT8223M)
Rev
1A
Date: Tuesday, February 22, 2011
Sheet 37 of 50

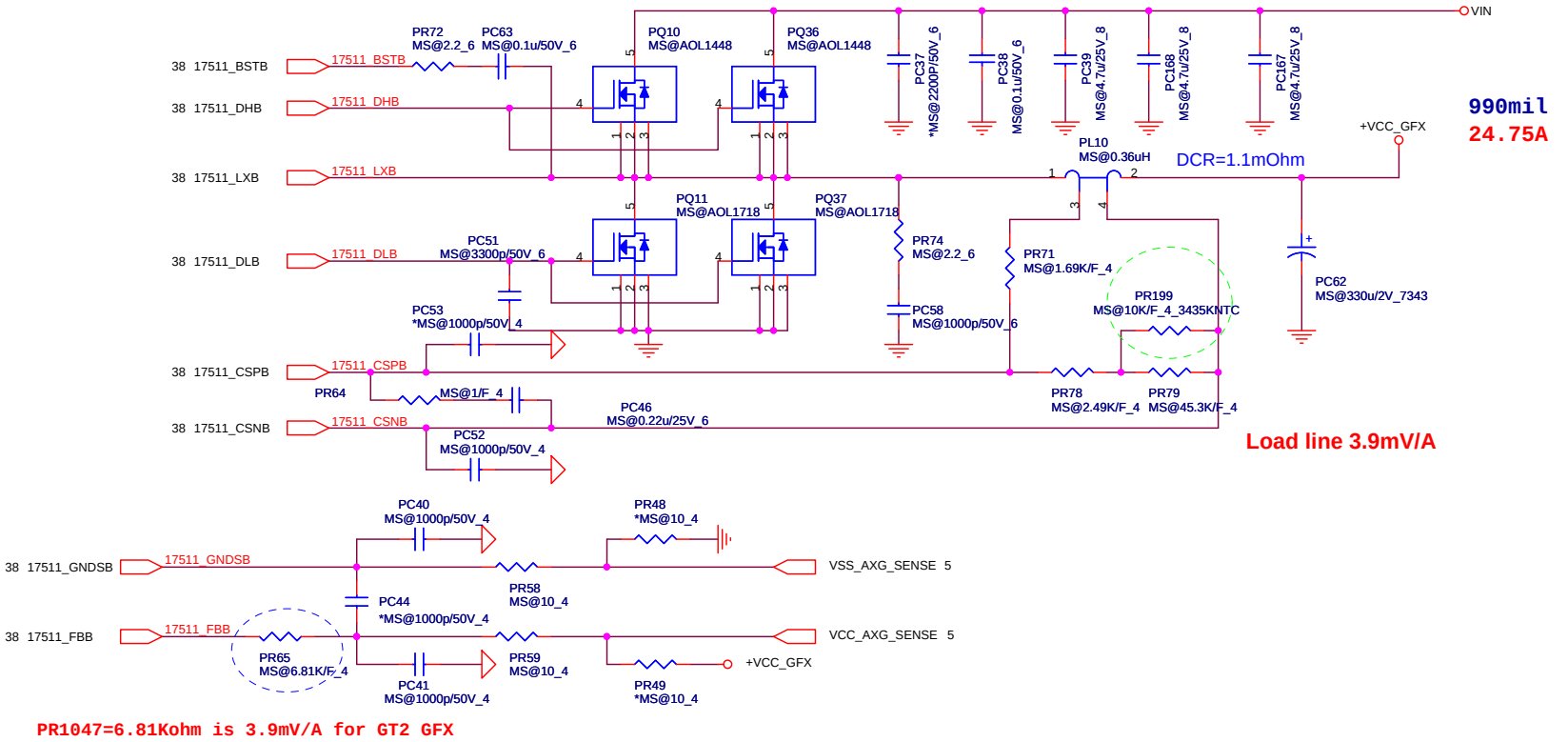


Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	+VCC_CORE (MAX17511))	1A

Date: Tuesday, February 22, 2011 Sheet 38 of 50



PR1047=6.81Kohm is 3.9mV/A for GT2 GFX

	Dual Core (35W)	Quad Core (45W)
CPU Conver	2-Phase	3-Phase
PR202	Populated	NC
PR95	150K/F_4 (CS41502FB18)	130K/F_4 (CS41302FB00)
PR94	200K/F_4 (CS42002FB12)	158K/F_4 (CS41582FB14)
PR111	NC	5.11K/F_4 (CS25112FB15)
PR100	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)
PR106	3.4K/F_4 (CS23402FB08)	5.11K/F_4 (CS25112FB15)

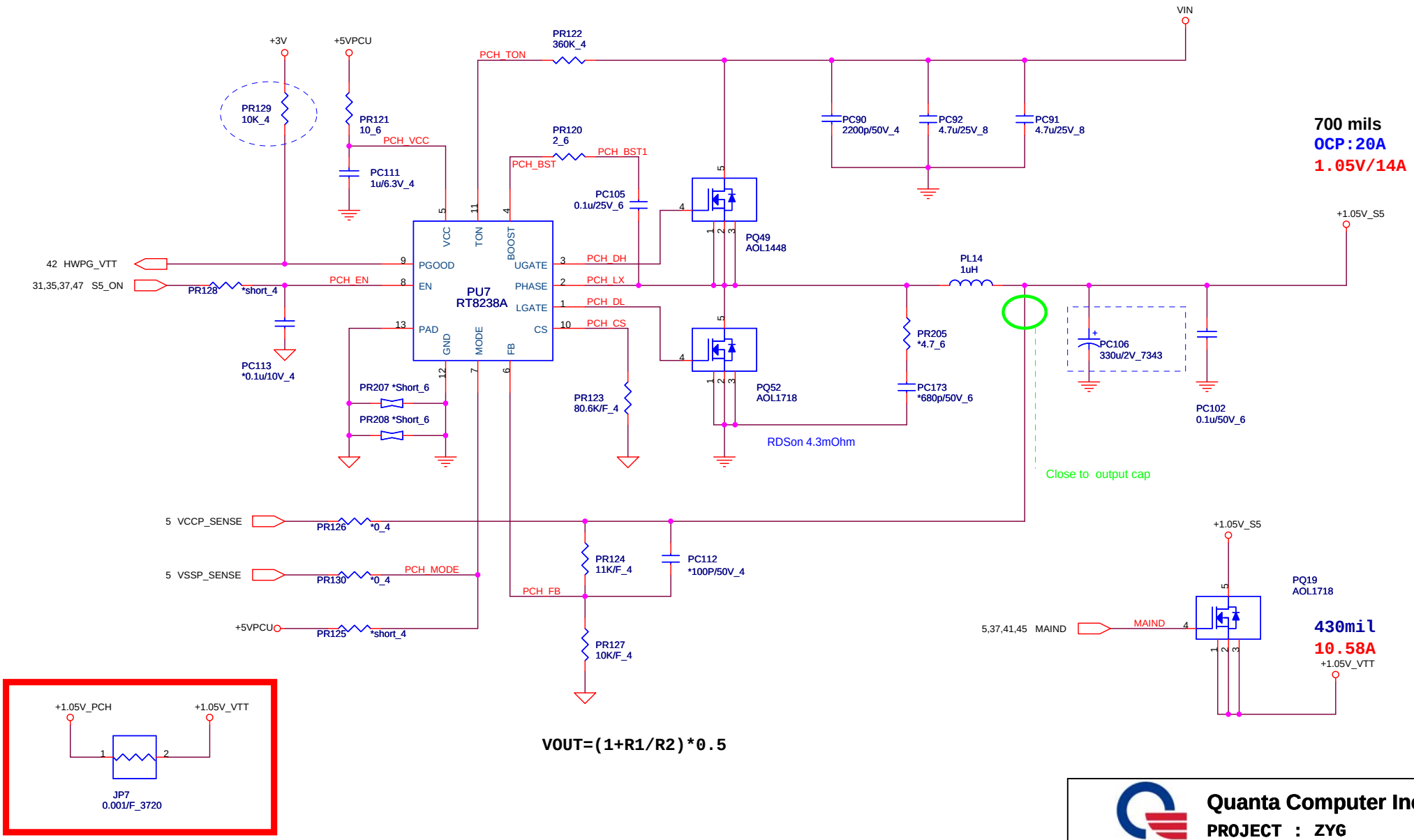
	UMA (IV@) / Muxless (MS@)	External VGA (EV@)
PR63	NC	Populated
PR67	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR91	130K/F_4 (CS41302FB00)	NC
PR90	158K/F_4 (CS41582FB14)	NC
PR88	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR69	Populated	NC
PR70	Populated	NC

Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	+VCC_GFX (MAX17511))	1A

Date: Tuesday, February 22, 2011 Sheet 39 of 50



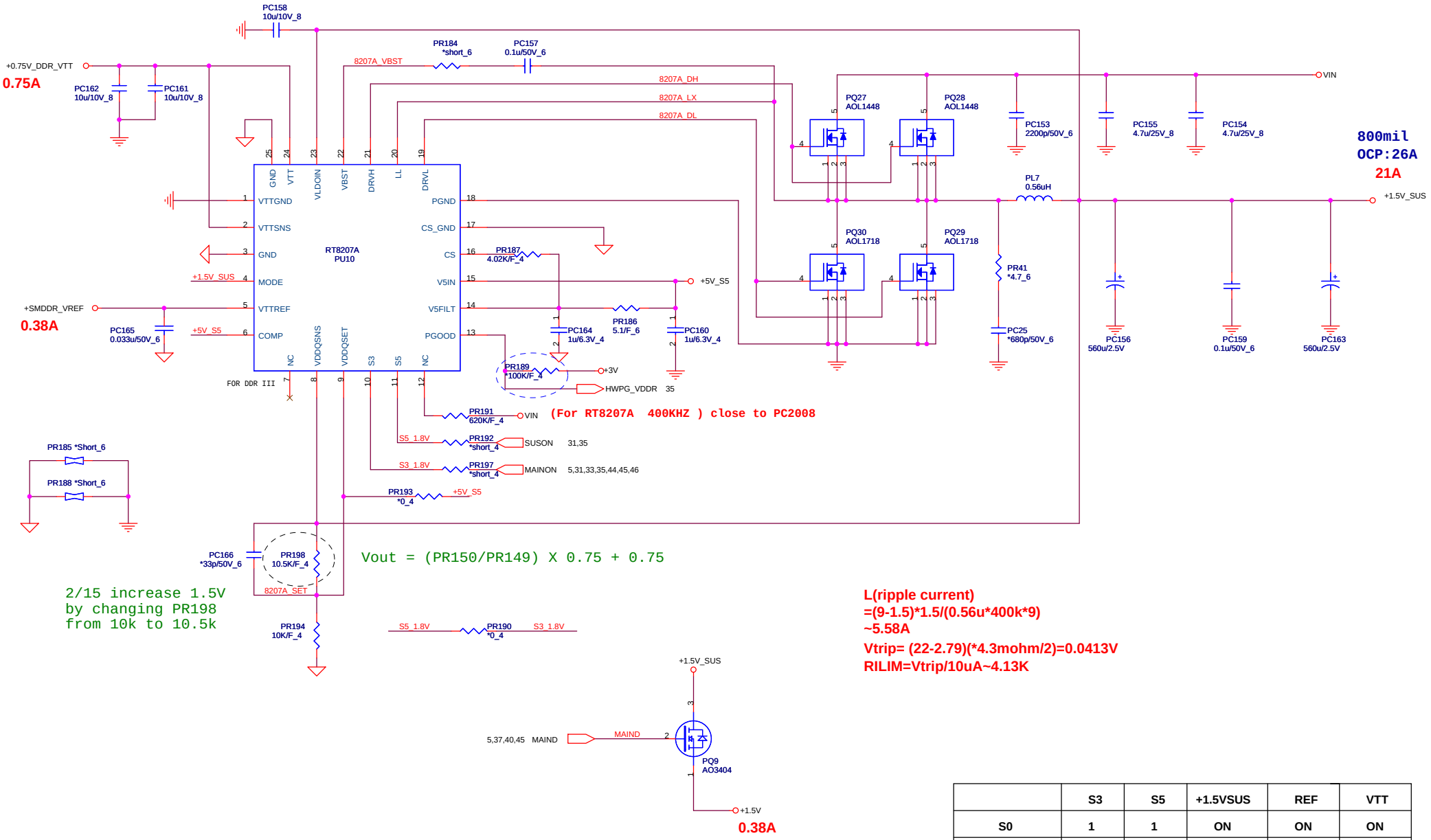
Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	+PCH&VTT (RT8238A)	1A

Date: Tuesday, February 22, 2011 Sheet 40 of 50

[PWM]



Vout = (PR150/PR149) X 0.75 + 0.75

2/15 increase 1.5V
by changing PR198
from 10k to 10.5k

L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

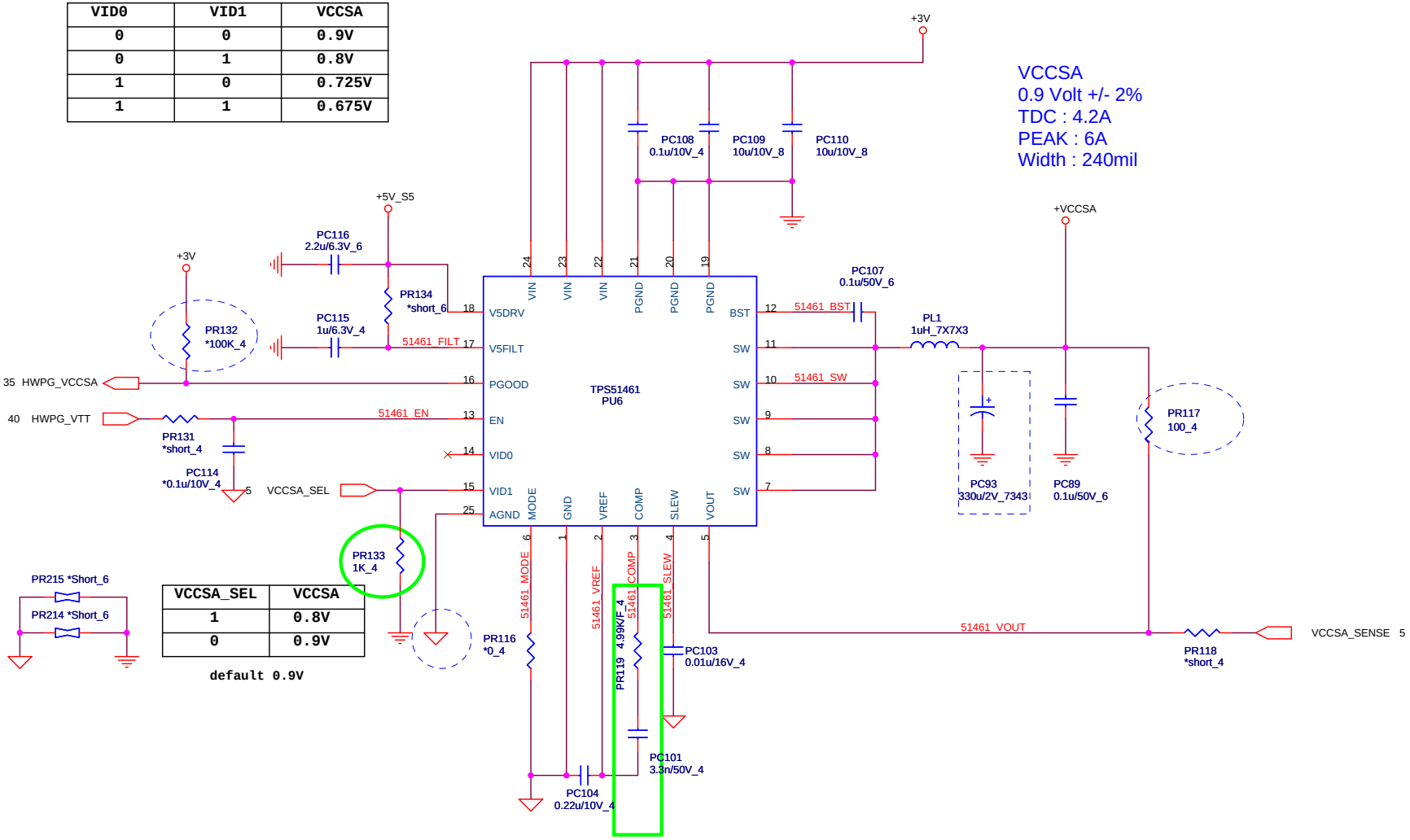
Quanta Computer Inc.
PROJECT : ZYG

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Tuesday, February 22, 2011 Sheet 41 of 50

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA
0.9 Volt +/- 2%
TDC : 4.2A
PEAK : 6A
Width : 240mil



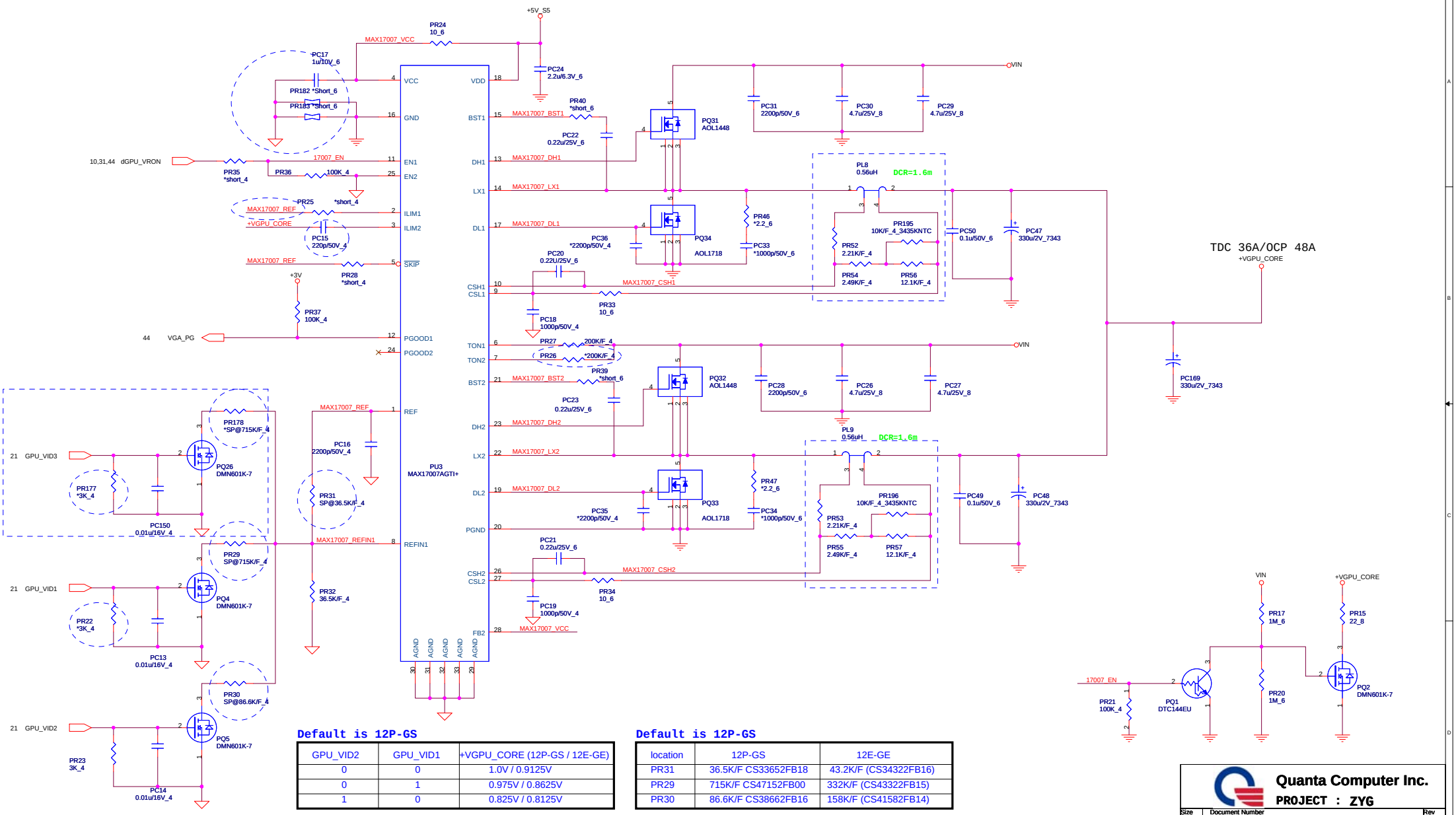
VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

Quanta Computer Inc.
PROJECT : ZYG

Size	Document Number	Rev
	VCCSA(TPS51461)	1A

Date: Tuesday, February 22, 2011 Sheet 42 of 50



Default is 12P-GS

GPU_VID2	GPU_VID1	+VGPU_CORE (12P-GS / 12E-GE)
0	0	1.0V / 0.9125V
0	1	0.975V / 0.8625V
1	0	0.825V / 0.8125V

Default is 12P-GS

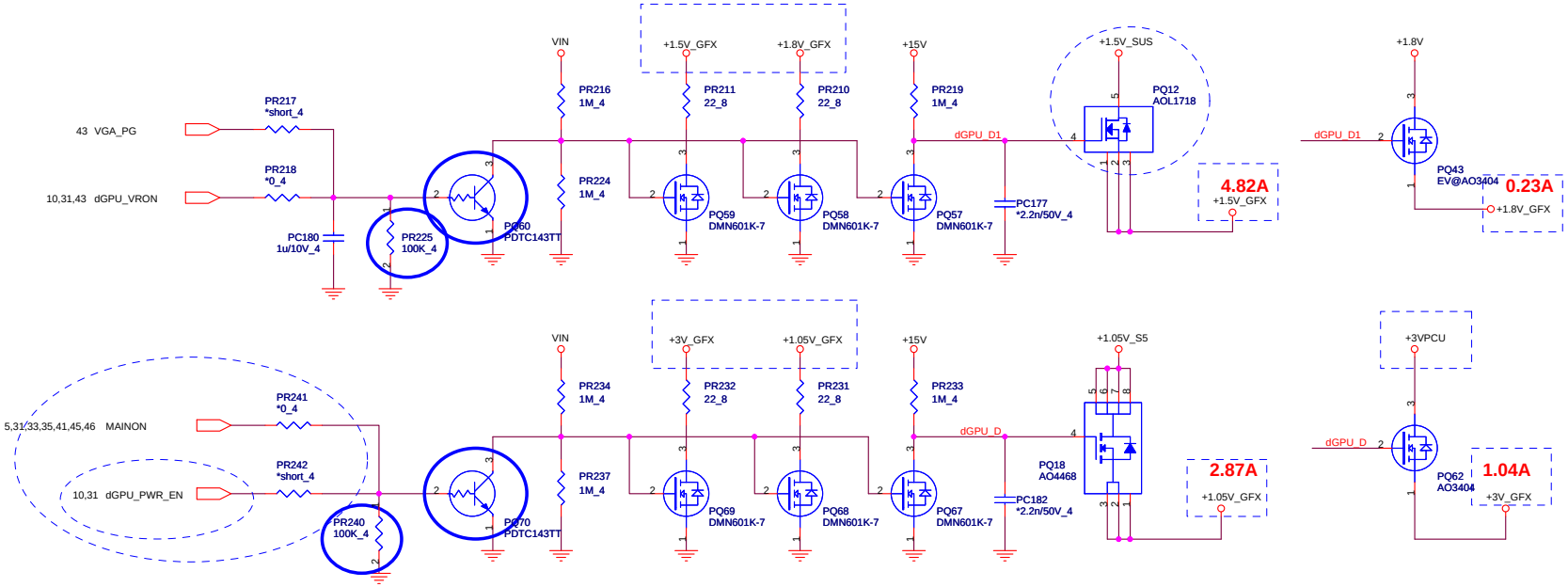
location	12P-GS	12E-GE
PR31	36.5K/F CS33652FB18	43.2K/F (CS34322FB16)
PR29	715K/F CS47152FB00	332K/F (CS43322FB15)
PR30	86.6K/F CS38662FB16	158K/F (CS41582FB14)

Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	GPU CORE(MAX17007)	1A

Date: Tuesday, February 22, 2011 Sheet 43 of 50



Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	GPU_PWR	1A

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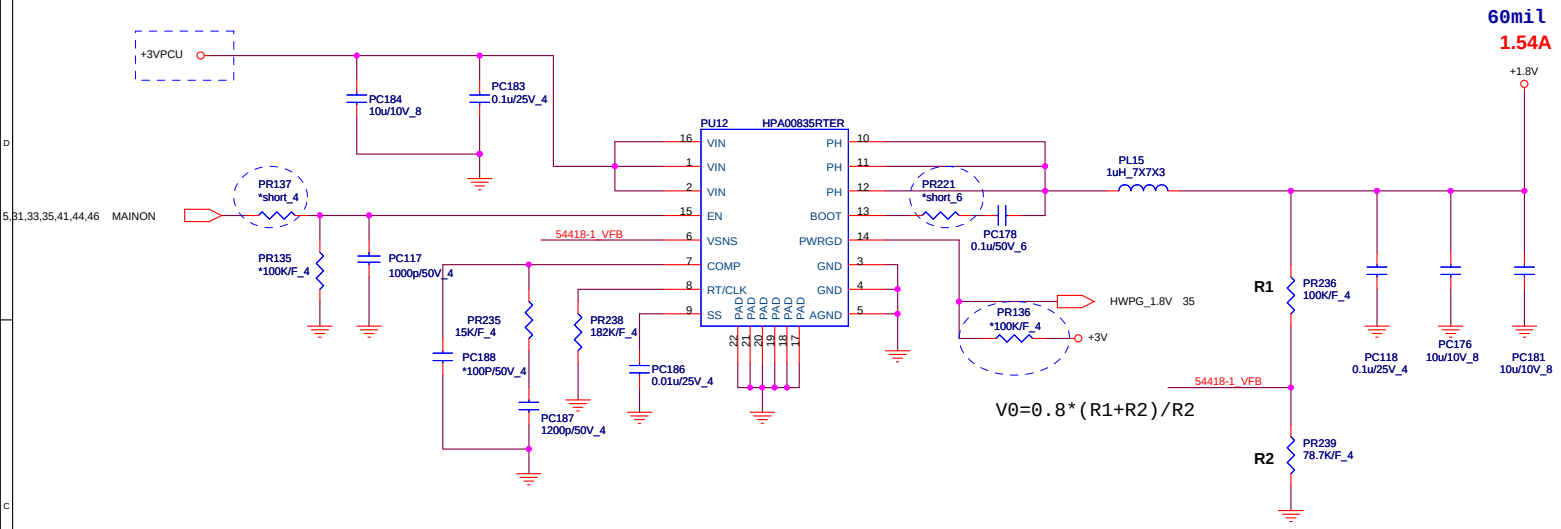
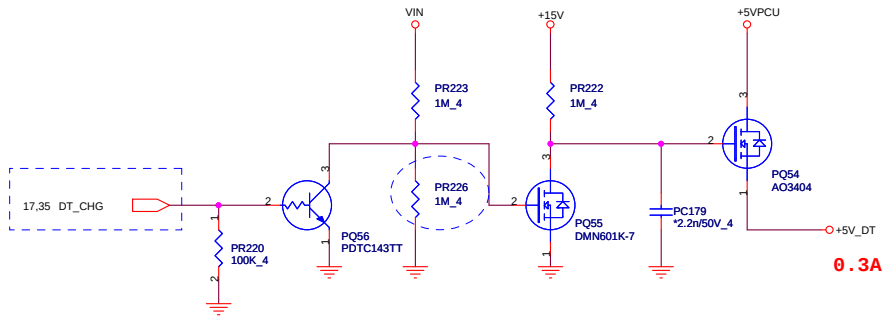
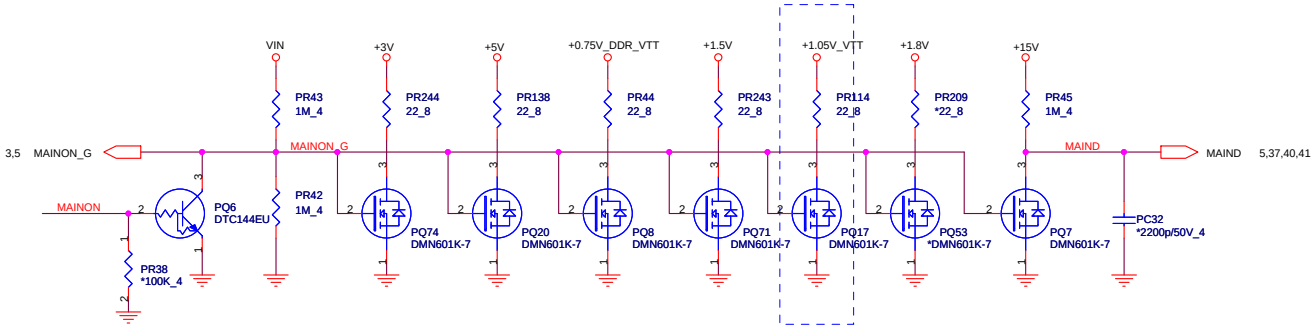




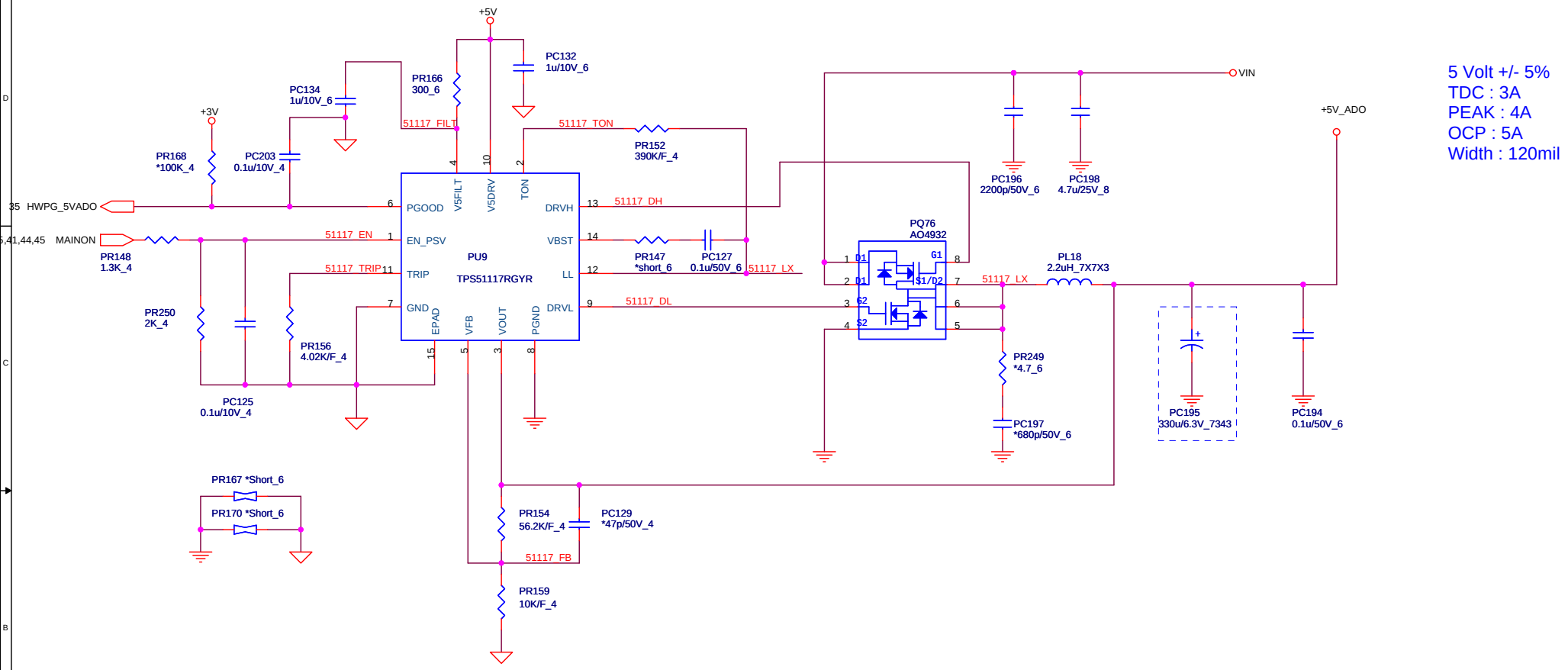


Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	+1V/+1.8V/Discharge	1A

Date: Tuesday, February 22, 2011 Sheet 45 of 50



5 Volt +/- 5%
TDC : 3A
PEAK : 4A
OCP : 5A
Width : 120mil

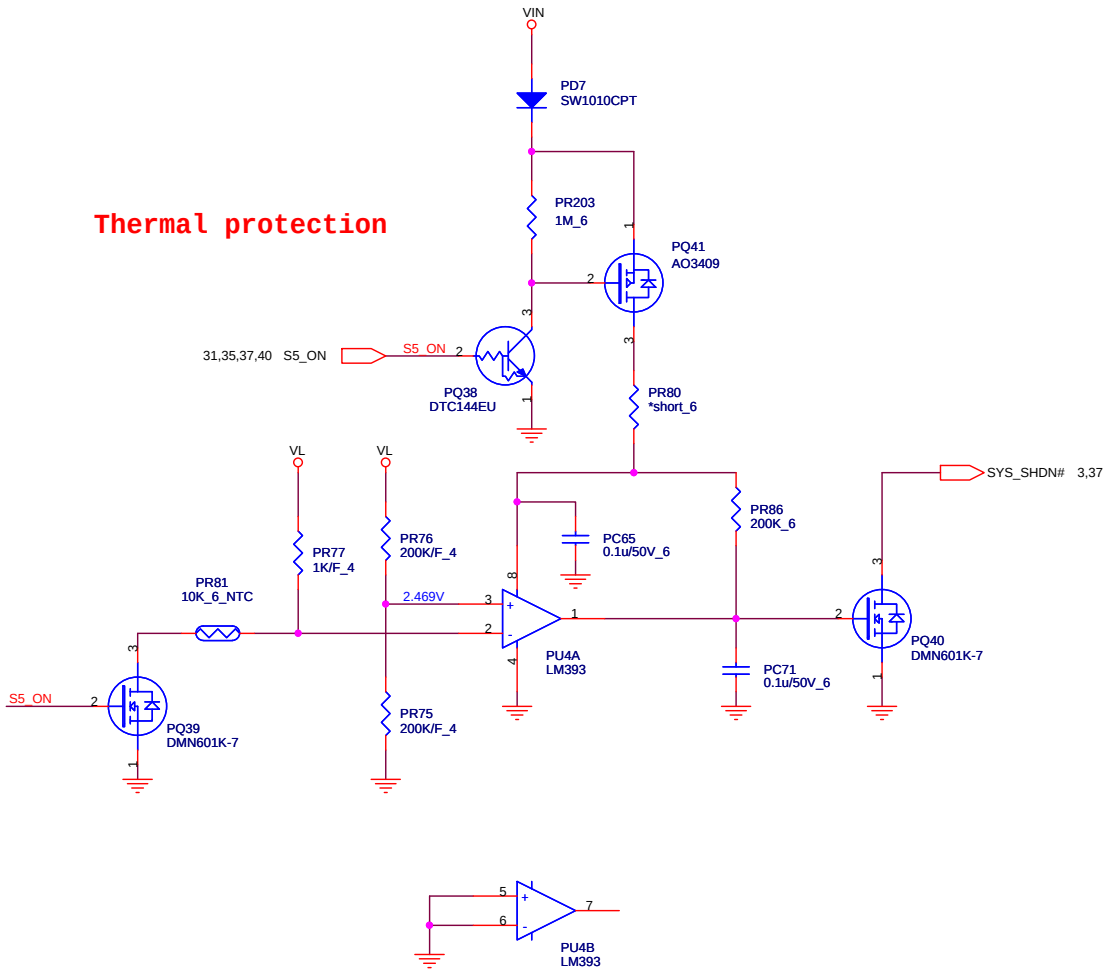
Quanta Computer Inc.

PROJECT : ZYG

Size	Document Number	Rev
	+5V_ADO (TPS51117)	1A

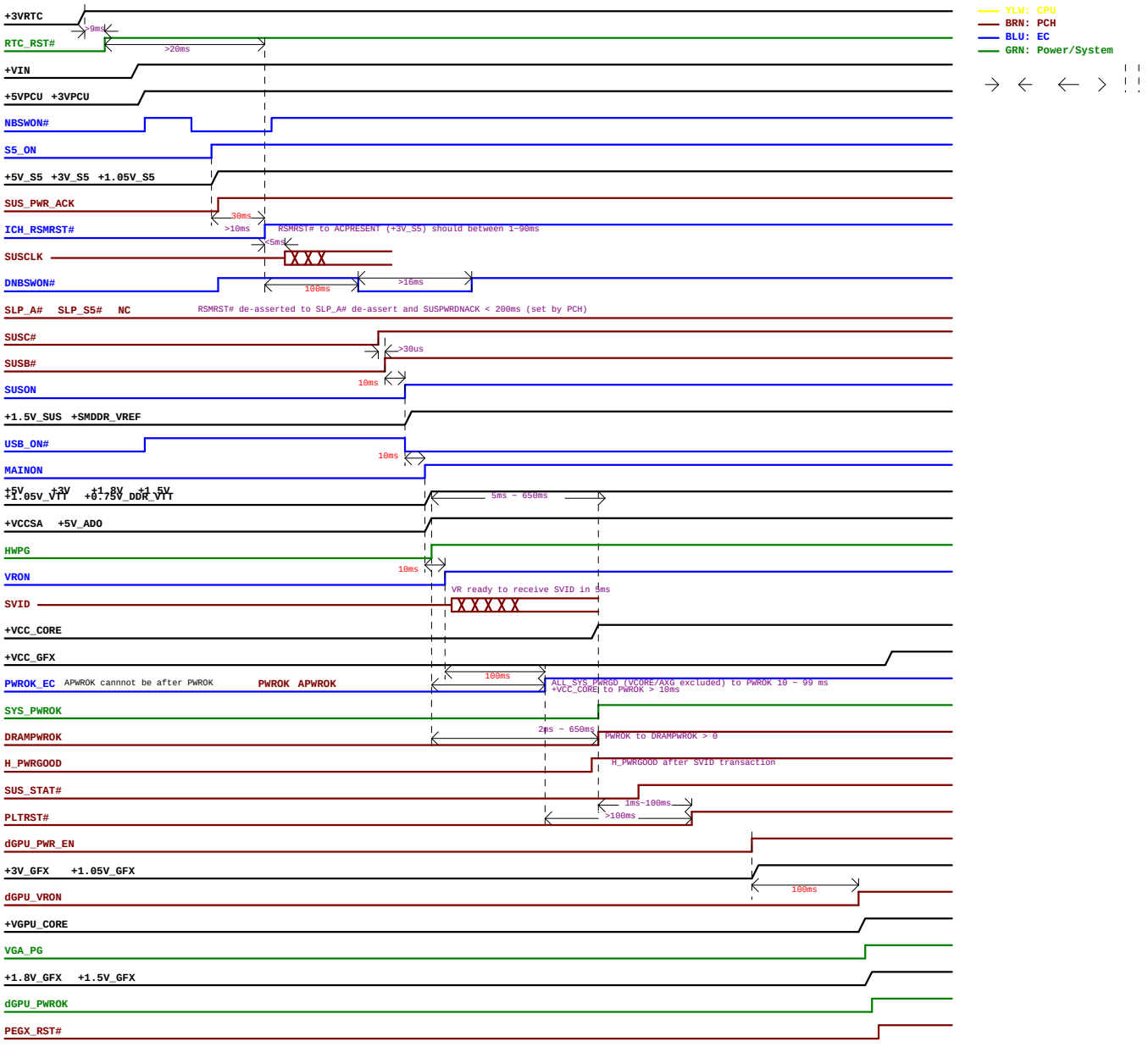
Date: Tuesday, February 22, 2011 Sheet 46 of 50

Thermal protection



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZYG		
Size	Document Number: Thermal protect	Rev 1A
Date: Tuesday, February 22, 2011	Sheet 47 of 50	



YLW: CPU
BRN: PCH
BLU: EC
GRN: Power/System

Title	<Title>	
Size	Document Number	Rev
Custom	<Doc>	1A
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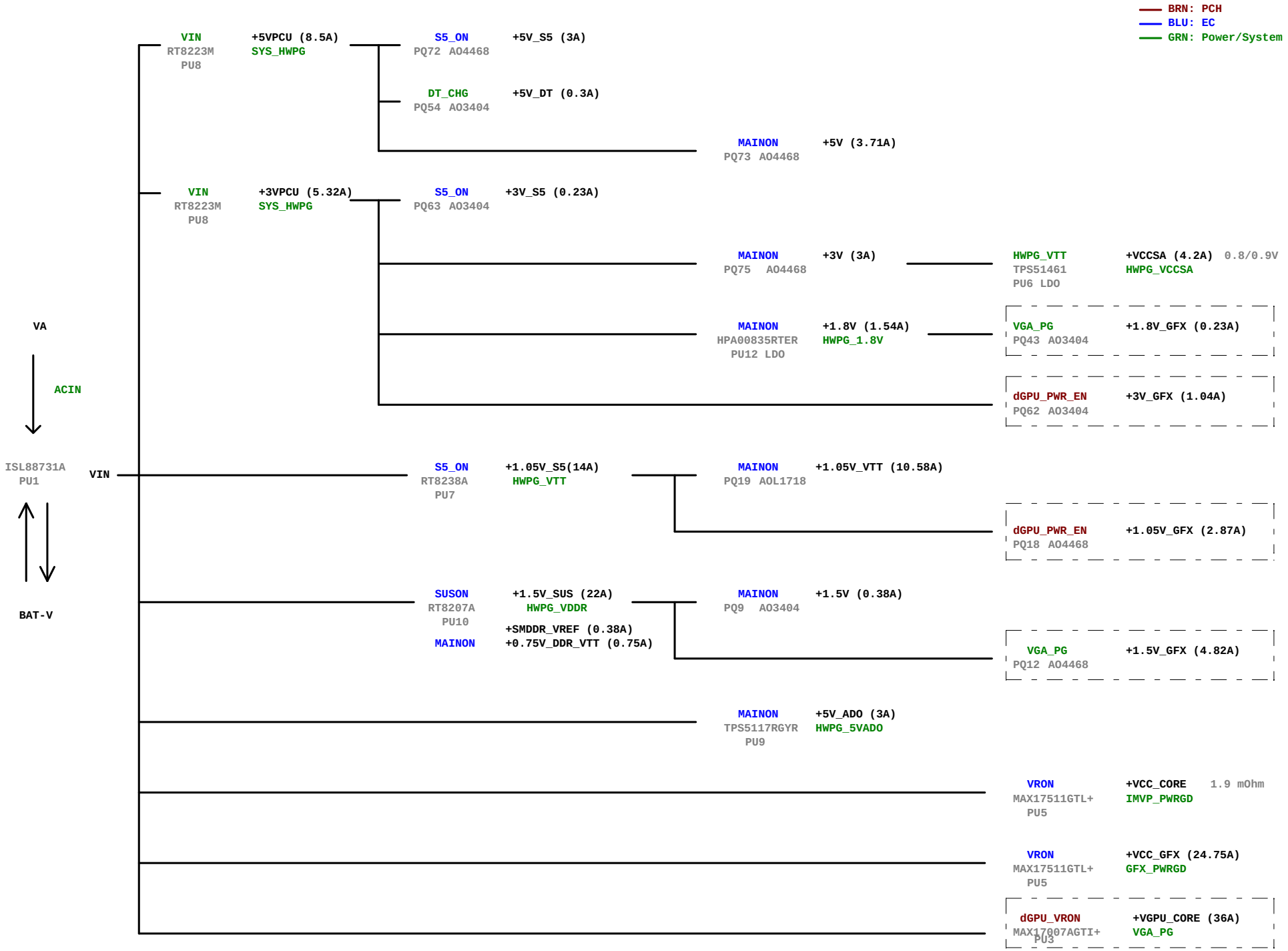

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Model

ZYG MB

CHANGE LIST

REV		TEXT
C	2010/12/28	Create ZYG C-stage schematics based on "ZYG_MB_REVB24_1220_FINAL.DSN"
		Rename net name SV_DET to BOARD_ID2 in page 10
	2010/01/05	Update part description with "ZYG_C_Desc_0105.upd"
		Change SW5 baterry reset switch PN and footprint
	2010/01/06	Change CN16 1394 connector footprint and pin assignment
	2010/01/10	Construct rev.C07 shcematics based on rev.C02
		Delete TP58, TP60
		Change TP7, TP17 footprint to TP3050
		Change Hole 19, 21, 20, 22, 23, 24, 25 footprint
	2010/01/11	Add R716, R719 (mounted) 717, 718 (unmounted) mount R155 and unmount U11, for EC controlling charger IC behavior
		Delete T6, R719, mount R718, U11, unmount R155, change netname ACPRN to USB3_POWER_ON to control USB charger and-gate
		Use crystal 24MHz clock for USB3.0: unmount R542, R549, R555, mount R556, Y2, C715, C717 on page 33; unmount R328 on page 9
		Mount Q42 for USB wake up function
		Change Q42 PN (for input 1.5 V > VIH 1.4V)
		Add R720 and connect between EC pin 20 and BATT_EN#
	2010/01/12	Change USB3_POWER_ON to EC pin 113, leaving pin 109 ACPRN and T6
		Add costdown solution with "C_costdown_0112.upd"
		Add buffers (U43, U44, Q46, D42, R721, R722, RV9, RV10,) to DT_ATTACH# and DT_CHG
		Add reserved 0.1uF C824 for ESD concern
		Merge SV_DET to BOARD_ID2
		Update power schematics
		Adjust R353 357 360 362 363 value for LED luminance
	2010/01/13	Adjust mounting and value for CPU AXG power with "Costback_0113.upd"
		Add 22 Ohm R723 between DT_ATTACH# and EC for ESD prevention
		Add RV11, reserved 100k R719, mount R246 and change from 10uF_6 to 22uF_8 in DT dongle power
		Change EC GPIO37 (pin72) reserved pull-high from +3V_S5 to +3VPCU
		Update capacitor descriptions and values with "DescUPD1.upd", "DescUPD2.upd", "DescUPD3.upd"
		Change R723 from 2.2 Ohm 0603 to 0 Ohm 0402
		Mount R719 100k
		Add R724 reserved 0 Ohm
	2010/01/14	Change 0 ohm R723 from 0402 to 0603
		Update 1394 CN16 PN to DFHS04FR511
C2	2010/01/25	Create ZYG C2-stage schematics based on "ZYG_MB_REVC_FINAL_GARY_UPD.DSN"
		Change DT connector/buffer ground as DTGND and connect to GND with R725 C825 C826
	2010/01/26	Left CN13 pin5,6 NC
		Change R725 from 0 ohm to CX08T301024 (EMI CHIP PBY160808T-301Y-N (300+-25%,2A))
	2010/01/27	Update TOP/BOT with "C2_topbot_0127.upd"
Ramp	2010/01/31	Create ZYG Ramp-stage schematics based on "ZYG_MB_REVC2_05_0127_GARY.DSN"
		Change and mount D22, D31 from CY5R5M10900(0603) to CY402V05B00(0402)
	2010/02/14	Unmount Q42 to disable S3 wakeup function for USB 3.0
		Change U40 from AJSLH9D0T02 to AJSLJ4P0T10
		Change SW5 PN to DHPATE2CK02
	2010/02/15	Change D31 back to CY5R5M10900(0603)
		Mount C822 for CRT
		Increase 1.5V by changing PR198 from 10k to 10.5k to avoid 3DMark running hangup
		Change L41, L42, L43 to CX8BA470003/CX8PG330007 for N12P/N12E
	2010/02/16	Update U36 to AL000547000 (USB power switch 2A)
		Change C13, C14 to CY402V05B00 (ESD varistor)
	2010/02/17	Change 0-Ohm to short pad with "RampShortPadUPD0217.upd"
		Delete L13, L7, L45, L10, L11, L12, L17, L14, L18
		Dismount PU2
		Change PQ12 from AO4468 to AOL1718
	2010/02/18	delete C826
		change C825 PN to BC040201Z00
		change U44 pin5 from +5V_DTPWR to +3VPCU
		rename net N129824580 to DT_CHG_R
		Add U45
		Dismount R725
		Add Q47
		Delete RV9, RV10, RV11
	2010/02/22	Change R694 from shortpad to 0 Ohm
		Change L3, L4 to CX5AG601001 (600 ohm, 300mA)
		Add pin7, 8 floating on CN13
		Delete TP33, change DT_GND to pin3 of U45, swap pin4, 6 of U45
		Rename N129824552 to DT_CHG#, add R726, Q48
		Delete Q48, R726; connect DT_CHG and DT_CHG# with R726 (0 ohm)
		Change R694 from 0 ohm to 22 ohm for EMI concern
		Update TOP/BOT with "TOPBOT_ramp0222.upd"
		Change R722 to 200k_4 (TOP)
		Mount C796 with 10p cap
	2010/02/23	Change Q47 to AOS3404 MOS (TOP)
		TEXT

Quanta Computer Inc.

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